Cascode Current Mirror

The main property/feature of a current source/sink is that the current though the device is independent of the voltage across it. Figure 1 shows the most basic of current sink. The current **Iout** is set by the voltage applied across the gate-source of the device, the greater the voltage the larger the current flow through the device. However as you can see from Figure 1 as the current increases then the slope in the saturation increases – for an ideal current sink/source we want this region to be flat ie very high resistance. These saturation slopes extrapolate to a point on the –x axis known as the Channel length modulation parameter λ, which is equal 1/-x, typical values are 0.01-0.05. The smaller this value then the smaller the slope in saturation and the better the current source/sink will be.

The output resistance r_{out} is given by:-
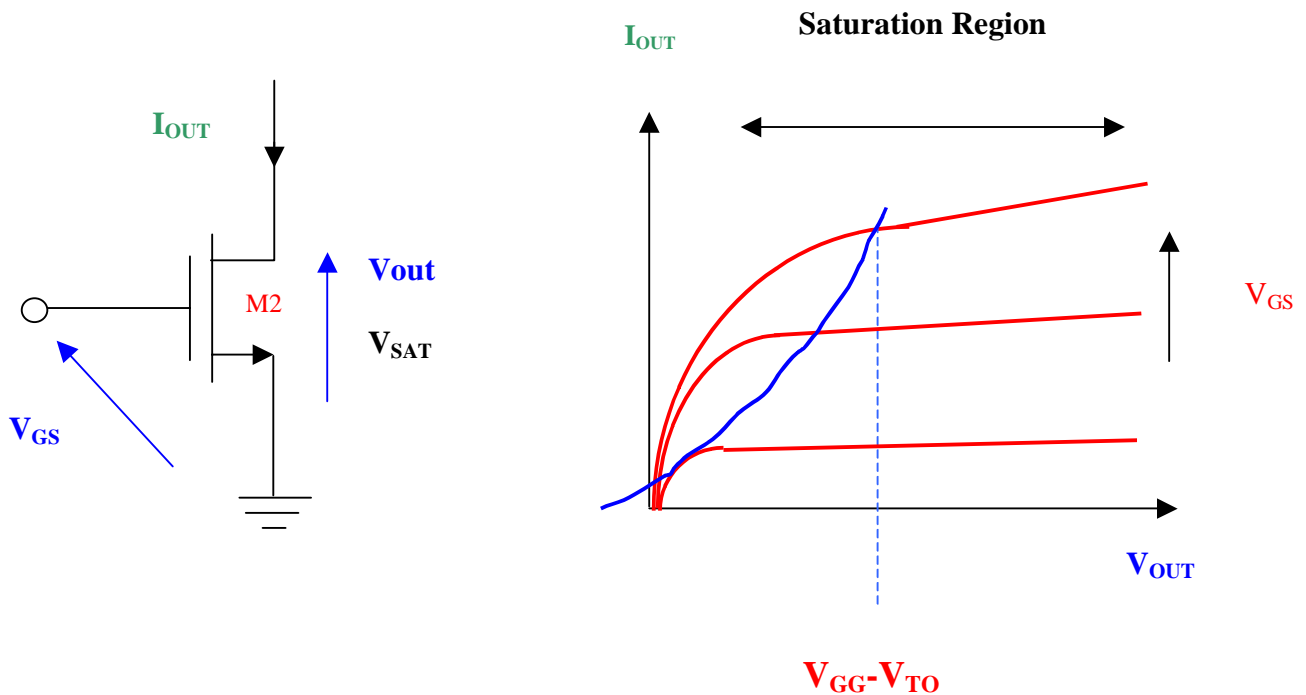
$$rout = \frac{1}{\lambda . I_D}$$

Figure 1 Simple current sink

As the slope in saturation region is determined by the output resistance r_{out} then increasing this will greatly improve the performance of the current source/sink. In addition we would like to reduce Vsat to allow larger voltage swings across the device.

One way of increasing the output resistance is to add a resistor between the source and ground as shown in Figure 2. In reality this method is not to practical because of the voltage drop across the resistor however, we can replace the resistor by an active resistor formed by a CMOS Fet and this forms the basis of the cascode current source/sink.
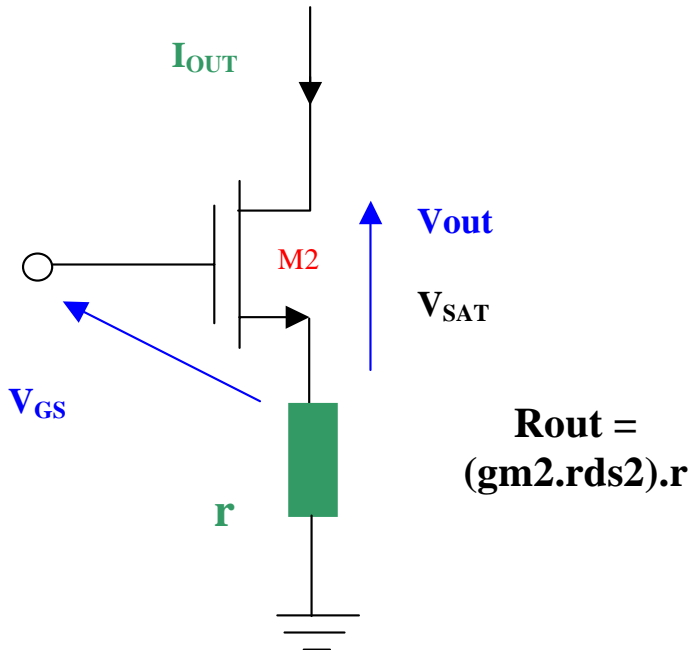
I_{OUT}

M2

V_{out}

V_{SAT}

V_{GS}

r

$$Rout = (gm2.rds2).r$$

Figure 2 Method for increasing performance of current source/sink by adding a source resistor to increase rout by (gm2.rds2)r.

I_{OUT}

V_{GS1}

M2

V_{out}

$2V_{SAT}$

V_{GS2}

M1

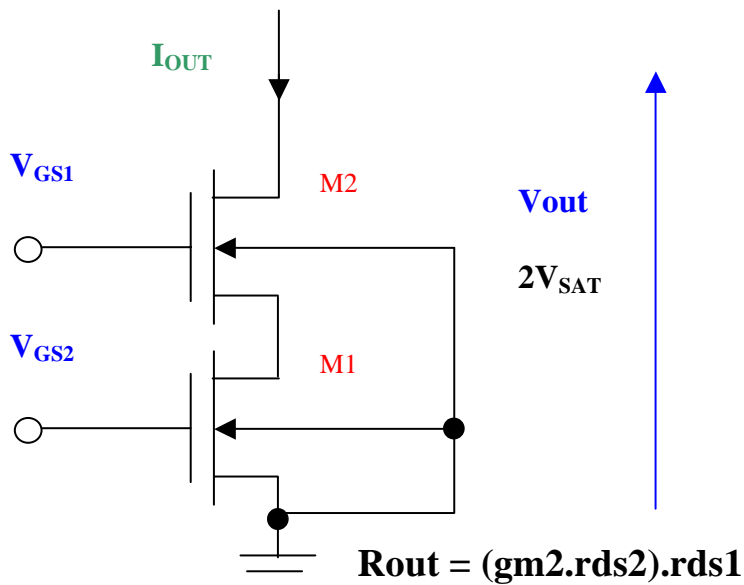$$Rout = (gm2.rds2).rds1$$

Figure 3 Adding an active load to increase the rout of the current source/sink to improve performance.

Figure 3 Shows the addition of an active load to M2 can increase the output resistance from rds2 to (gms2.rds2).rds1.

MOS Diode

When the gate and drain terminals are connected together on a CMOS FET the operation is similar to a p-n junction diode. The circuits for the n-type and p-type diode (active resistors) are shown in Figure 4.
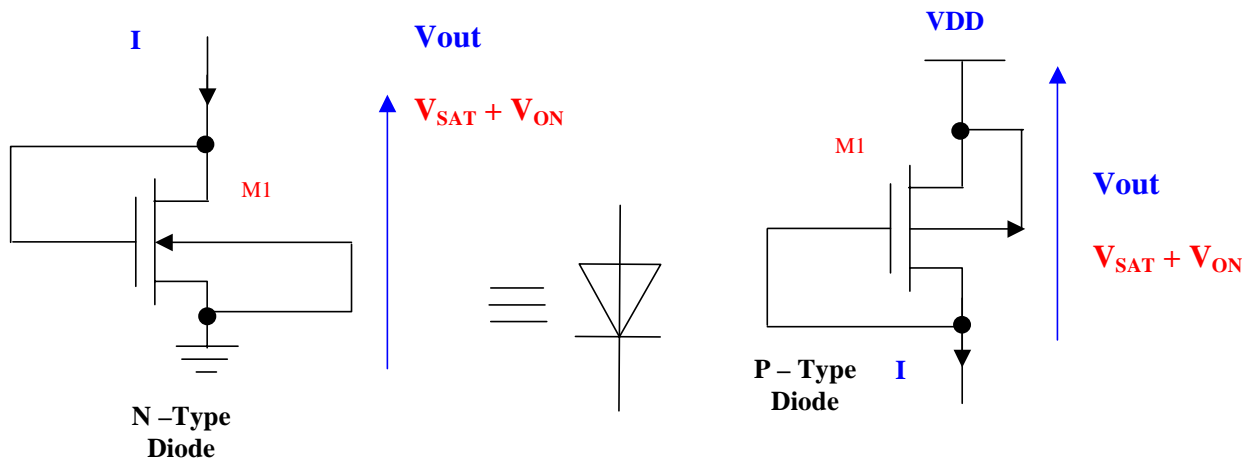

Figure 4 Active resistor/diode configurations. The gates are connected to the drains, and the sources are connected to supplies.

As used as an active load the resistance of the 'diode' is **1/gm**.

$$I_D = \frac{\beta}{2}(V_{GS} - V_T)^2 \quad \text{Where} \quad \beta = \frac{K'W}{2L}$$

As in the diode configuration the gate is connected to the source then $V_{GS} = V_{DS}$

$$\text{and } I_D = \frac{\beta}{2}(V_{DS} - V_T)^2 \quad \text{rearrange to get VDS}$$

$$\text{VDS} = \sqrt{\frac{2I_D}{\beta}} + V_T$$

In most applications these diodes can be used to generate a fixed bias voltages as shown in Figure **5**.

VDD

M2

Vout2

$2V_{SAT} + 2V_{ON}$

I

M1

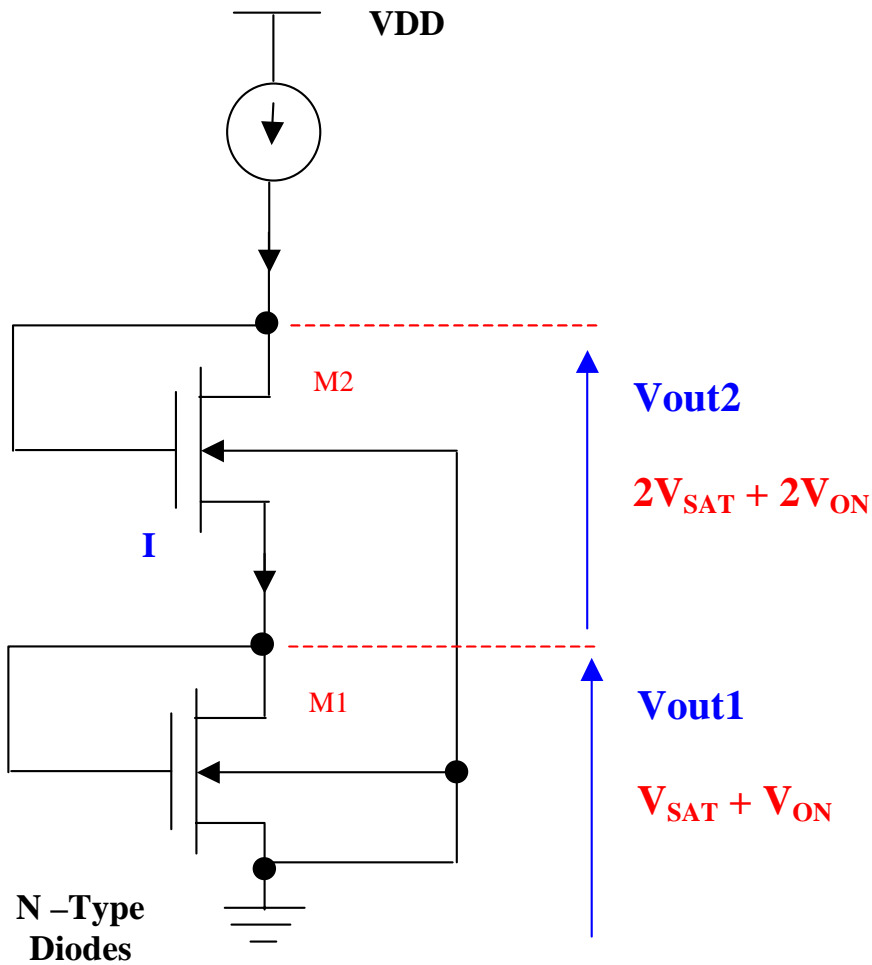Vout1

$V_{SAT} + V_{ON}$

N –Type Diodes

Figure 5 Two N-type CMOS diodes giving two fixed bias voltages of $V_{SAT}+V_{ON}$ and $2_{VAT}+2_{VON}$

We can use these CMOS diodes to provide bias to the current mirror shown in Figure 3 to form the most popular current source/sink circuits known as the cascode current mirror

M1 & M2 are effectively two diodes in series with a total voltage drop of $2V_{SAT}+2_{VT}$, which is fairly independent of current I_{REF}. I_{REF} can be set using a resistor or band-gap/resistor network.
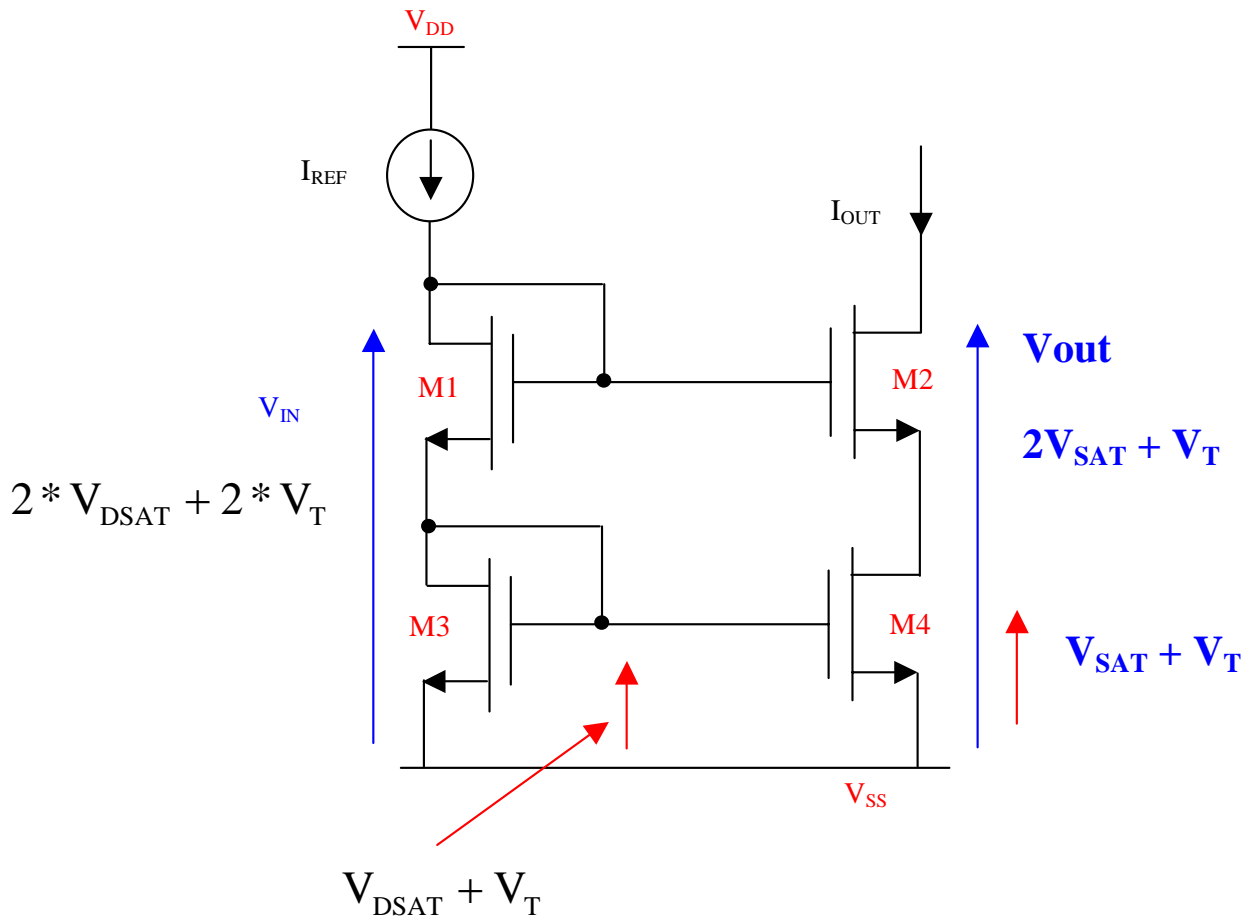
Figure 6 Cascode current source, showing that the minimum voltage output is 2V$_{SAT}$+V$_T$ above the rail VSS (in this case 0V). M1 and M3 are wired as diodes and each have a voltage drop of V$_{SAT}$+V$_T$ across the drain-source junction.

This circuit has higher output impedance than the simple current mirror, but lower output swing due to the extra device.

$$V_D \geq V_G - V_T \qquad - (1)$$

The bias to M2 (Vgs2) is $2V_{SAT} + 2_{VT}$ Sub into (1)

$$V_D \geq (2V_{SAT} + 2V_T) - V_T \; = \; 2V_{SAT} - V_T$$

$$R_{IN} = \frac{1}{gm_1} + \frac{1}{gm_3}$$

$$R_{OUT} = \frac{gm_2}{go_2 \cdot go_4} \; = \; gm.r_{ds}^2$$

Example

Using the circuit of Figure 6, with VDD = +5V and VSS = -5V. Assuming the following parameters V_T = 1V, Kp = 80E-6, λ = 0.02. Calculate Vgs, Vout and Rout. All FETs are the same (W/L =1).

$$Vgs = V_T + \sqrt{\frac{I_{REF}}{Kp}} \quad = \quad 1 + \sqrt{\frac{20E^{-6}}{80E^{-6}}} \quad = \quad 1.5V$$

$$V_{SAT} = V_{GS} - V_T \quad = \quad 1.5 - 1 = 0.5$$

$$V_{out} = VSS - (2V_{SAT} + V_T) \quad = \quad 5 - 2(0.5) + 1 = -3V$$

$$R_{OUT} = R_{O4} + R_{O2}(1 + gm4.R_{O4})$$

$$gm = \frac{2.I_D}{V_{GS} - V_T} \quad = \quad \frac{2 * 20E^{-6}}{1.5 - 1} \quad = \quad 80E^{-6} A/V$$

$$R_{O4} = R_{O2} = \frac{1}{\lambda.I_D} \quad = \quad \frac{1}{0.02 * 20E^{-6}} = 2.5M\Omega$$

$$\therefore R_{OUT} = 2.5E^6 + 2.5E^6(1 + 80E^{-6}.2.5E^6) = 505M\Omega$$

The above circuit with the data given was simulated in ADS using a DC simulation to verify the calculated results. The simulation setup is shown in Figure 7, for this setup the circuit was analysed and the **annotate DC solution** selected to add all the node voltage and currents to the circuit.

www.rfic.co.uk

DC
DC
DC1
SweepVar=
Start=0
Stop=5
Step=.01

Var
Eqn
VAR
VAR2
W=1
VDD=5
L=1
LAMBDA=0.02

MOSFET_NMO
MOSFET3
Model=MOSFETM
Length=L um
Width=W um
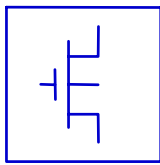
LEVEL1_Mode
MOSFETM
NMOS=yes
Vto=1
Kp=80e-6
Lambda=LAMBD

-40.0 uA

V_DC
SRC2
Vdc=VDD

R
R1
R=400000

-20.0 uA

20 uA

I_DC
SRC1
Idc=20 uA

20 uA

-20.0 uA

20.0 uA

-2.98 V
vd4

I_Probe
I1

-1.61 V
vgs3

-5.11 pA   0 A   0 A   -3.63 pA

S   S

-20 uA   -20.0 uA

MOSFET_NMO
MOSFET4
Model=MOSFETM
Length=L um
Width=W um

20 uA

-3.41 V
vd1

-20.0 uA

-5 V

MOSFET_NMO
MOSFET2
Model=MOSFETM
Length=L um
Width=W um

20 uA

-3.30 V
vgs2

-5 V 1.71 pA   0 A   0 A   -1.60 pA

-5 V   -5 V S   -5 V S -5 V

-5 V

-20 uA   -5 V   40.0 uA 5 V   -20.0 uA

MOSFET_NMO
MOSFET1
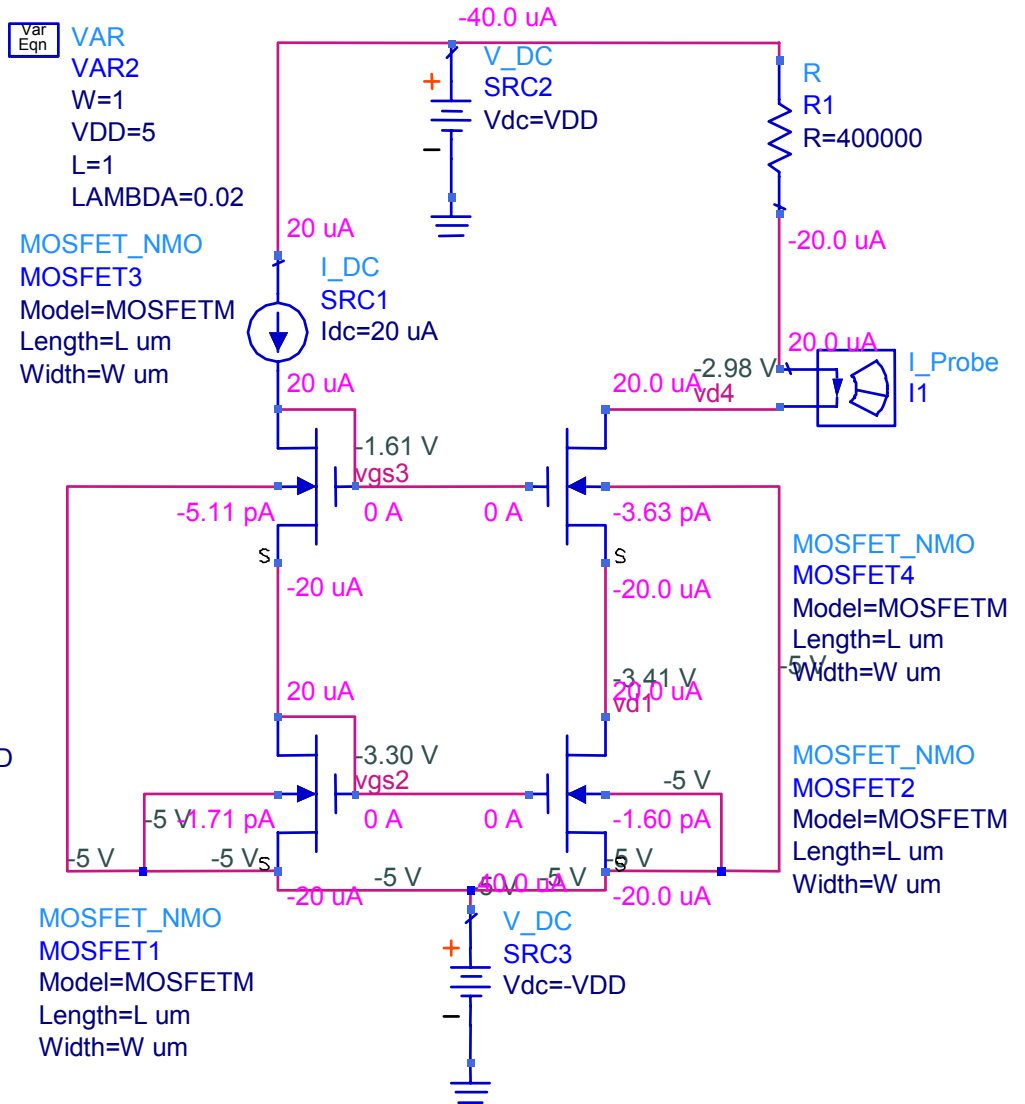Model=MOSFETM
Length=L um
Width=W um

V_DC
SRC3
Vdc=-VDD

Figure 7 ADS DC simulation of the cascode current source example. The resistor load has been calculated assuming a current of 20uA and a Vout minimum of –3V. NOTE that the bulk connections have been connected to the lowest circuit potential ie –VDD or –5V. The simulation has given slightly different results from the simplified hand calculations as you would expect.

Decreasing VOUT

A cascode current sink can be used in the 'tail' in a long-tail pair/differential amplifier to improve the common mode rejection. However, because we are using two stages the current mirror will reduce the rail voltage available by $V_{OUT} = 2V_{SAT} + V_T$, which could be typically ~ 2V less than the supply rail. Other cascode circuits have been modified to reduce V_{OUT} as much as possible.

One such circuit is shown in Figure 8.

$$V_{GS} = V_{ON} + V_T$$

So rearranging $V_{ON} = V_{GS} - V_T$ is also $= V_{SAT}$

$$Id = \frac{K'W}{2L}(V_{GS} - V_T)^2 \quad \text{we can sub in to get} \quad Id = \frac{K'W}{2L}(V_{ON})^2$$

And $V_{ON} = \sqrt{\dfrac{2.Id.L}{K'W}}$

If we set the W/L ratio of M1 to 0.25 then

$$V_{ON} = \sqrt{\frac{2.Id.4W}{K'L}} = \sqrt{4} = 2.V_{ON}$$

Therefore, Vgs1 is **$V_T + 2V_{ON}$**

$V_D \geq V_G - V_T \qquad - \quad (1)$

To bias to M2 (Vgs1) is $2V_{SAT} + V_T$ Sub into (1)

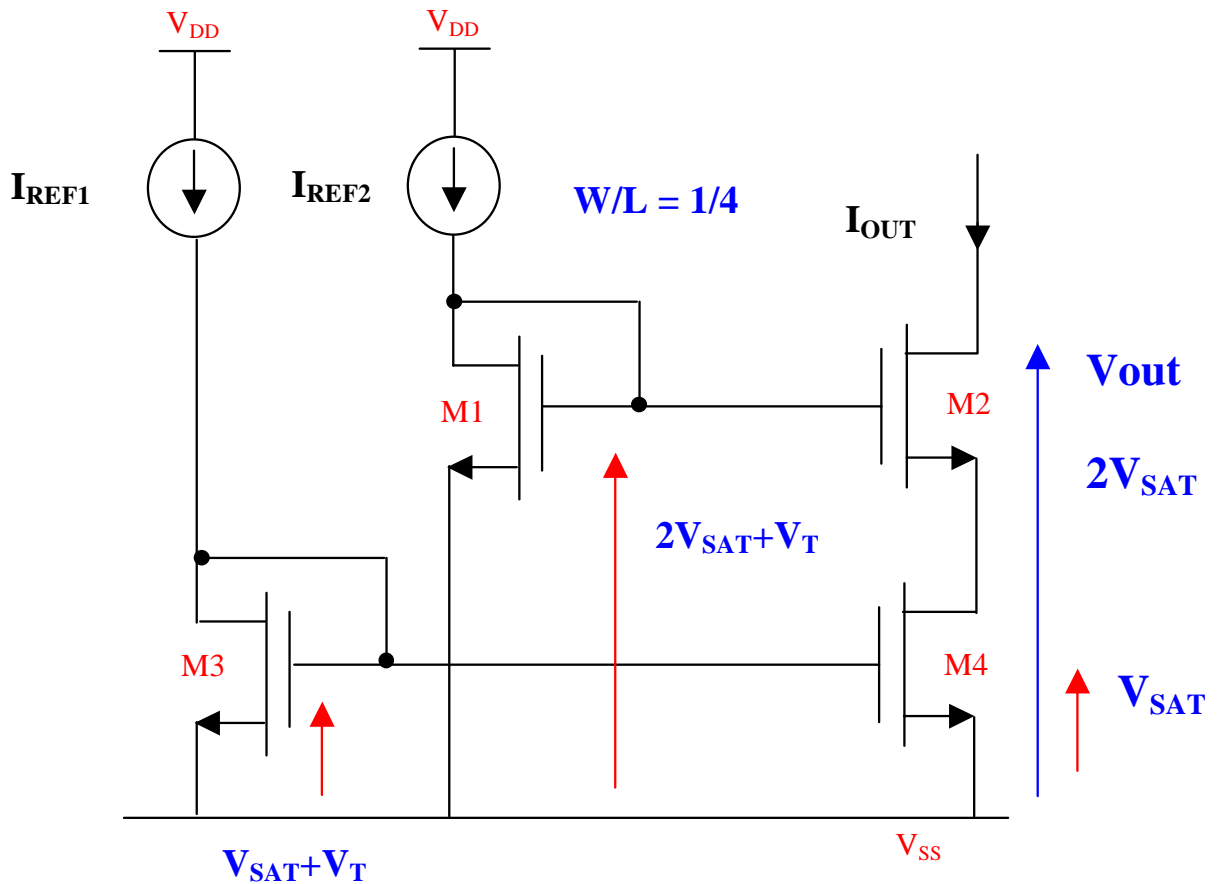$V_D \geq (2V_{SAT} + V_T) - V_T = $ **$2V_{SAT}$**

Figure 8 Method for decreasing the voltage drop across the two output devices to give a greater available voltage swing.

Although this circuit has a low output voltage drop (2VON) it suffers in that M1 connected to M2 are not matched devices (M1 has a W/L ratio of 0.25). As a result I_{OUT} will not track I_{REF} over temperature.

To eliminate this problem the circuit shown in Figure 9 is used.

Each pair of FETS in the cascode are fed with the same bias. M3 supplied $2V_{SAT}+V_T$ to the top pair FETS M4 and M5.

Figure 9 ADS Transient simulation of the improved high-voltage swing version of the cascode current source. The Vout in this case is –3.73V giving voltage across the two output FETs of 1.27V (giving a V_{ON} for each device of 0.635V).

射 频 和 天 线 设 计 培 训 课 程 推 荐

易迪拓培训(www.edatop.com)由数名来自于研发第一线的资深工程师发起成立，致力并专注于微波、射频、天线设计研发人才的培养；我们于 2006 年整合合并微波 EDA 网(www.mweda.com)，现已发展成为国内最大的微波射频和天线设计人才培养基地，成功推出多套微波射频以及天线设计经典培训课程和 ADS、HFSS 等专业软件使用培训课程，广受客户好评；并先后与人民邮电出版社、电子工业出版社合作出版了多本专业图书，帮助数万名工程师提升了专业技术能力。客户遍布中兴通讯、研通高频、埃威航电、国人通信等多家国内知名公司，以及台湾工业技术研究院、永业科技、全一电子等多家台湾地区企业。

易迪拓培训课程列表：http://www.edatop.com/peixun/rfe/129.html

射频工程师养成培训课程套装

该套装精选了射频专业基础培训课程、射频仿真设计培训课程和射频电路测量培训课程三个类别共 30 门视频培训课程和 3 本图书教材；旨在引领学员全面学习一个射频工程师需要熟悉、理解和掌握的专业知识和研发设计能力。通过套装的学习，能够让学员完全达到和胜任一个合格的射频工程师的要求…

课程网址：http://www.edatop.com/peixun/rfe/110.html

ADS 学习培训课程套装

该套装是迄今国内最全面、最权威的 ADS 培训教程，共包含 10 门 ADS 学习培训课程。课程是由具有多年 ADS 使用经验的微波射频与通信系统设计领域资深专家讲解，并多结合设计实例，由浅入深、详细而又全面地讲解了 ADS 在微波射频电路设计、通信系统设计和电磁仿真设计方面的内容。能让您在最短的时间内学会使用 ADS，迅速提升个人技术能力，把 ADS 真正应用到实际研发工作中去，成为 ADS 设计专家…

课程网址： http://www.edatop.com/peixun/ads/13.html

HFSS 学习培训课程套装

该套课程套装包含了本站全部 HFSS 培训课程，是迄今国内最全面、最专业的 HFSS 培训教程套装，可以帮助您从零开始，全面深入学习 HFSS 的各项功能和在多个方面的工程应用。购买套装，更可超值赠送 3 个月免费学习答疑，随时解答您学习过程中遇到的棘手问题，让您的 HFSS 学习更加轻松顺畅…

课程网址：http://www.edatop.com/peixun/hfss/11.html

CST 学习培训课程套装

该培训套装由易迪拓培训联合微波 EDA 网共同推出，是最全面、系统、专业的 CST 微波工作室培训课程套装，所有课程都由经验丰富的专家授课，视频教学，可以帮助您从零开始，全面系统地学习 CST 微波工作的各项功能及其在微波射频、天线设计等领域的设计应用。且购买该套装，还可超值赠送 3 个月免费学习答疑…

课程网址：http://www.edatop.com/peixun/cst/24.html

HFSS 天线设计培训课程套装

套装包含 6 门视频课程和 1 本图书，课程从基础讲起，内容由浅入深，理论介绍和实际操作讲解相结合，全面系统的讲解了 HFSS 天线设计的全过程。是国内最全面、最专业的 HFSS 天线设计课程，可以帮助您快速学习掌握如何使用 HFSS 设计天线，让天线设计不再难…

课程网址：http://www.edatop.com/peixun/hfss/122.html

13.56MHz NFC/RFID 线圈天线设计培训课程套装

套装包含 4 门视频培训课程，培训将 13.56MHz 线圈天线设计原理和仿真设计实践相结合，全面系统地讲解了 13.56MHz 线圈天线的工作原理、设计方法、设计考量以及使用 HFSS 和 CST 仿真分析线圈天线的具体操作，同时还介绍了 13.56MHz 线圈天线匹配电路的设计和调试。通过该套课程的学习，可以帮助您快速学习掌握 13.56MHz 线圈天线及其匹配电路的原理、设计和调试…

详情浏览：http://www.edatop.com/peixun/antenna/116.html

我们的课程优势：

※ 成立于 2004 年，10 多年丰富的行业经验，

※ 一直致力并专注于微波射频和天线设计工程师的培养，更了解该行业对人才的要求

※ 经验丰富的一线资深工程师讲授，结合实际工程案例，直观、实用、易学

联系我们：

※ 易迪拓培训官网：http://www.edatop.com

※ 微波 EDA 网：http://www.mweda.com

※ 官方淘宝店：http://shop36920890.taobao.com