Cascode CMOS Circuit

The cascode is a combination of a common-source device with a common-gate load. This has the effect of increasing the output impedance but minimises the Miller effect making it an ideal configuration for use at high frequencies. The circuit of the cascode amplifier is shown in Figure 1.

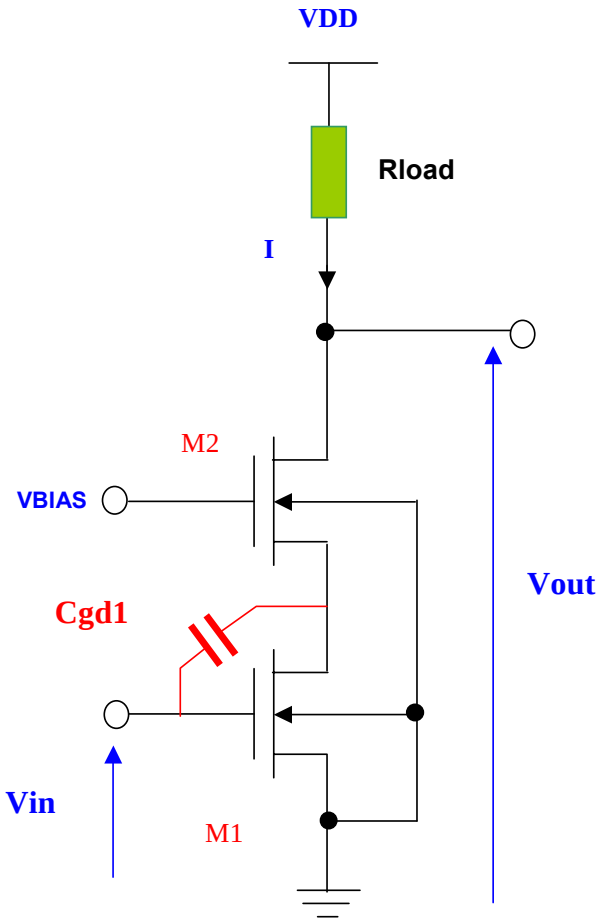


Figure 1 Basic Cascode Amplifier

Lets assume that FET M2 has a short between the drain and source terminals, the remaining circuit will be a common-source amplifier with a gain of:

$$Av = gm_1.R_{LOAD} \text{ or } \frac{gm_1}{g_{load}} \text{ strictly speaking } Av = \frac{gm1}{go_{load} + go_1}$$

Now miller effect occurs when there is a large impedance applied to the drain of the common-source M1 in this case it's R_{LOAD} but it could also be an active load with an even higher resistance. This has the effect of applying a gate shunt capacitance which, has a value of the M1 gate-drain capacitance multiplied by the voltage gain of the amplifier:-

$$C_{gate\text{-}shunt} = C_{gd1}(1+(gm_1.R_{LOAD}))$$

Thus with a particular source impedance connected to the input of the amplifier the 3-dB break point will be:-

$$f_{3dB} = \frac{1}{2\pi.Rs[C_{gs} + C_{gd1}(1+(gm_1.R_{LOAD}))]}$$

If there is a load capacitor attached to the load then a second higher frequency pole will be introduced:

$$f_{3dB} = \frac{Go_{LOAD}}{2\pi.C_{LOAD}} \quad \text{If } Go_{LOAD} \text{ is active then}$$

$$f_{3dB} = \frac{I_D(\lambda._{M1} + \lambda._{M2})}{2\pi.C_{LOAD}} \equiv \frac{1}{R_{LOAD}.2\pi.C_{LOAD}}$$

The M1 device is a voltage controlled source and the small gate voltage (Vgs) creates a large current (Ids) through the R_{LOAD} creating an output voltage (Vo) much greater than the input (Vgs) ie it has voltage gain. So if you could place a low impedance current buffer between M1 and the R_{LOAD} you could greatly reduce the Miller effect – and this is exactly what M2 biased into saturation does. The resistance looking into a source is pretty low:-

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{Vgs}{g_{M1}Vgs} = \frac{1}{g_{M1}} = I_D\lambda_{M2}$$

For a typical device @ 100uA, $\lambda = 0.01$ $R_{IN} = 1E-6\Omega$

A practical cascode amplifier is shown in Figure 2.

The device M2 acts as a low impedance current buffer, isolating the amplifying M1 with the load M3. Therefore, the gain of the cascode amplifier is approximately:-

$$Av = \frac{gm_1}{go_3} \text{ strictly speaking } Av = \frac{gm_1}{go_3 + go_1}$$

$$Av = -\sqrt{\frac{2.K_{N1}.W_1}{L_1.I_D.\lambda_3}}$$

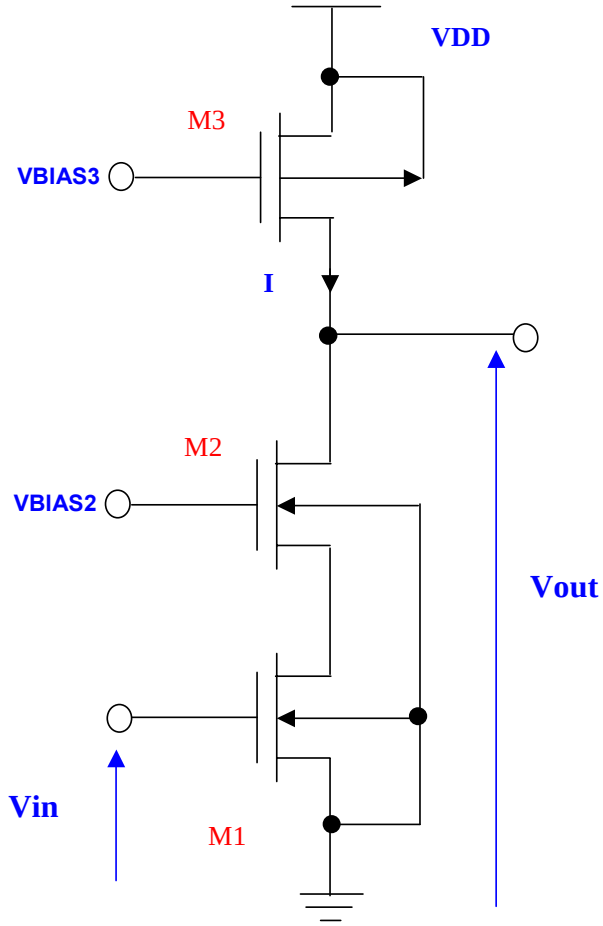


Figure 2 Cascode amplifier with active load

$$R_{OUT} \cong rds_3 = \frac{1}{I_D \lambda_3}$$

To be able to fully characterise the amplifier we need expressions in order to calculate output voltage swing and frequency response.

$$V_{OUTMAX} = VDD - VDS_{3SAT}$$

$$V_{OUTMIN} = \frac{\beta_{M3}}{2.\beta_{M2}}\left(VDD - VBIAS3 - |VT3|^2\right)\left(\frac{1}{VBIAS2 - VT2} + \frac{1}{VDD - VT1}\right)$$

$$\text{Where } \beta = \frac{K.W}{L}$$

Example

Determine the gain, output resistance, gate bias voltages, Vmax and Vmin of the cascode amplifier of Figure 2. Assume W=L=1um, K_N=110uA/V^2, K_P=50uA/V^2, λ = 0.05; V_T = 0.7V, ID=100uA.

The first step is to calculate the required bias voltages for each device.

First set the correct current to 100uA, so we need to determine the correct vgs to apply to the N-type FET.

$$Vgs = V_T + \sqrt{\frac{I_{REF}}{K_N}} = 0.7 + \sqrt{\frac{100E^{-6}}{110E^{-6}}} = 1.65V$$

$$V_{SAT} = V_{GS} - V_T = 1.65 - 0.7 = 0.95V$$

So we set the amplifying device M1 to vgs = 1.65V and the second device to Vgs+V_{SAT} = 2.6V.

And set the correct Vgs to apply to the P-type FET active source.

$$Vgs = V_T + \sqrt{\frac{I_{REF}}{K_P}} = +0.7 + \sqrt{\frac{100E^{-6}}{50E^{-6}}} = 0.72V \text{ (apply } 5 - 0.7 = 4.3V \text{ to gate terminal)}$$

So we set the bias to M3 at 4.3V.

Calculation of gain

$$Av = \frac{gm_1}{go_3} \text{ strictly speaking } Av = \frac{gm_1}{go_3 + go_1}$$

$$Av = -\sqrt{\frac{2.K_{N1}.W_1}{L_1.I_D.\lambda_3}} = -\sqrt{\frac{2.110E^{-6}.1E^{-6}}{1E^{-6}.100E^{-6}.0.05}} = 6.63 = 16.5dB$$

Output Resistance

$$R_{OUT} \cong rds_3 = \frac{1}{I_D\lambda_3} = \frac{1}{100E^{-6}.0.05} = 200K\Omega$$

Output Voltage Swing

$$V_{OUTMAX} = VDD - VDS_{3SAT}$$

$$VDS_{3SAT} = V_{GS3} - V_{T3} = 0.72 - 0.7 = 0.02V$$

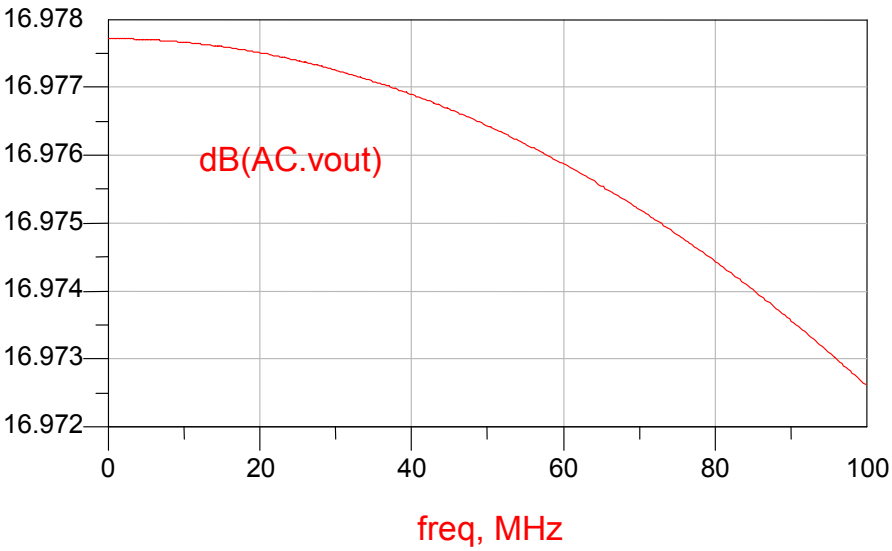
$$V_{OUTMAX} = 5 - 0.02 \cong 5V$$

$$V_{OUTMIN} = \frac{\beta_{M3}}{2.\beta_{M2}}\left(VDD - VBIAS3 - |VT3|^2\right)\left(\frac{1}{VBIAS2 - VT2} + \frac{1}{VDD - VT1}\right)$$

$$\text{Where } \beta = \frac{K.W}{L}$$

$$V_{OUTMIN} = \frac{\frac{50E^{-6}.1}{1}}{2.\frac{110E^{-6}.1}{1}}\left(5 - 3.9 - |0.7|^2\right)\left(\frac{1}{2.35 - 0.7} + \frac{1}{5 - 0.7}\right) = 0.227.(0.61)(0.838) = 0.116V$$

The ADS simulation of the example cascode is shown in Figure 4. The gain plot as a result of the simulation is shown in Figure 3.



DC.IDS.i	DC.VSAT_N	DC.vout
95.59uA	699.3mV	1.397 V

Figure 3 Resulting Gain plot from the ADS simulation of the example Cascode Amplifier

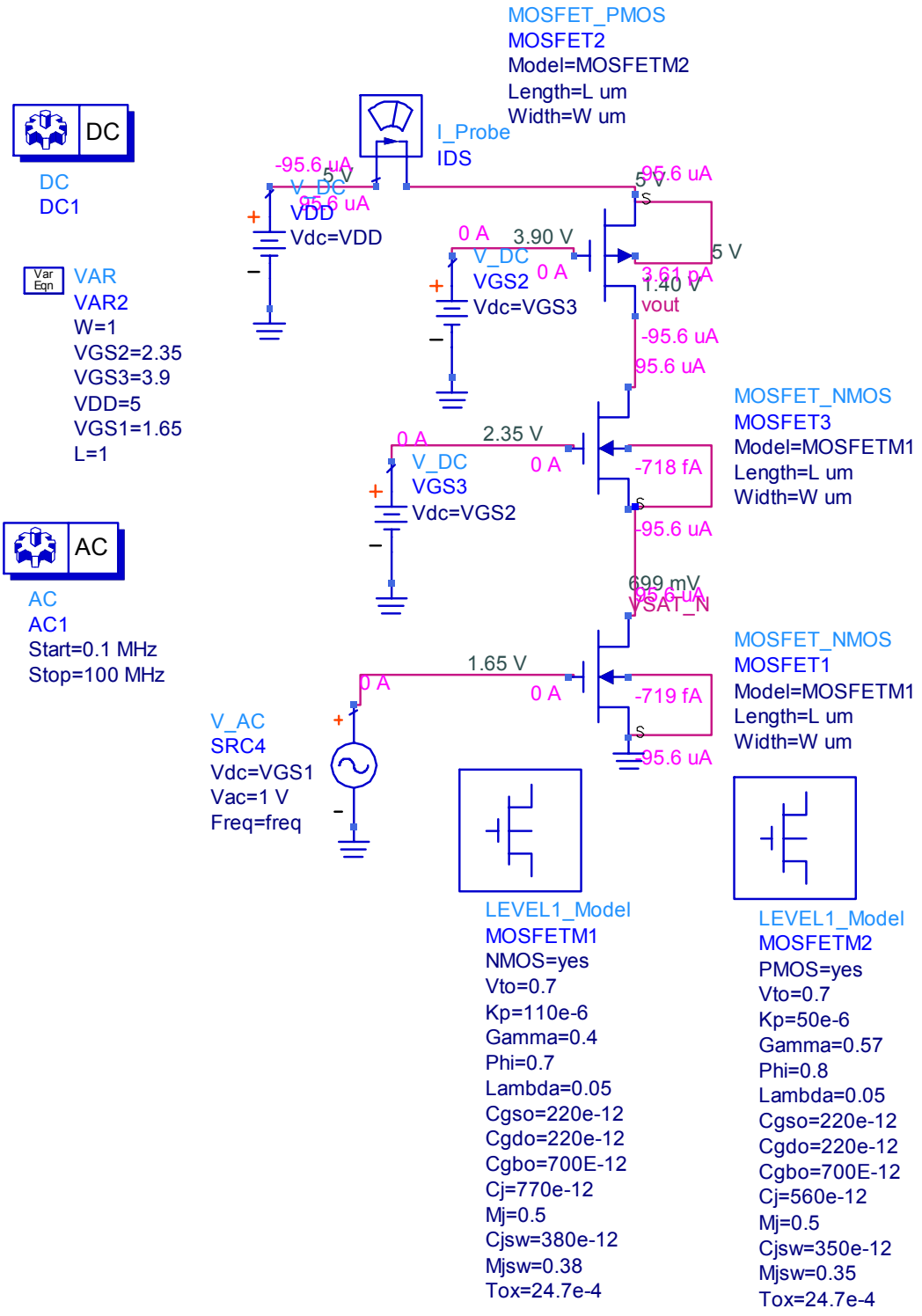


Figure 4 ADS simulation setup for the example Cascode Amplifier

A more practical circuit is shown in Figure 5. This circuit now includes the correct bias current mirrors and associated bias setting resistor. The left hand bias arm includes FETs configured as diodes such that the voltage across each source-drain is $V_{SAT}+V_T$. One advantage of doing

this is that the voltage drop across the resistor is smaller and therefore requires a smaller bias resistor, in this case about 1K which can easily be formed from a Polysilicate printed resistor.

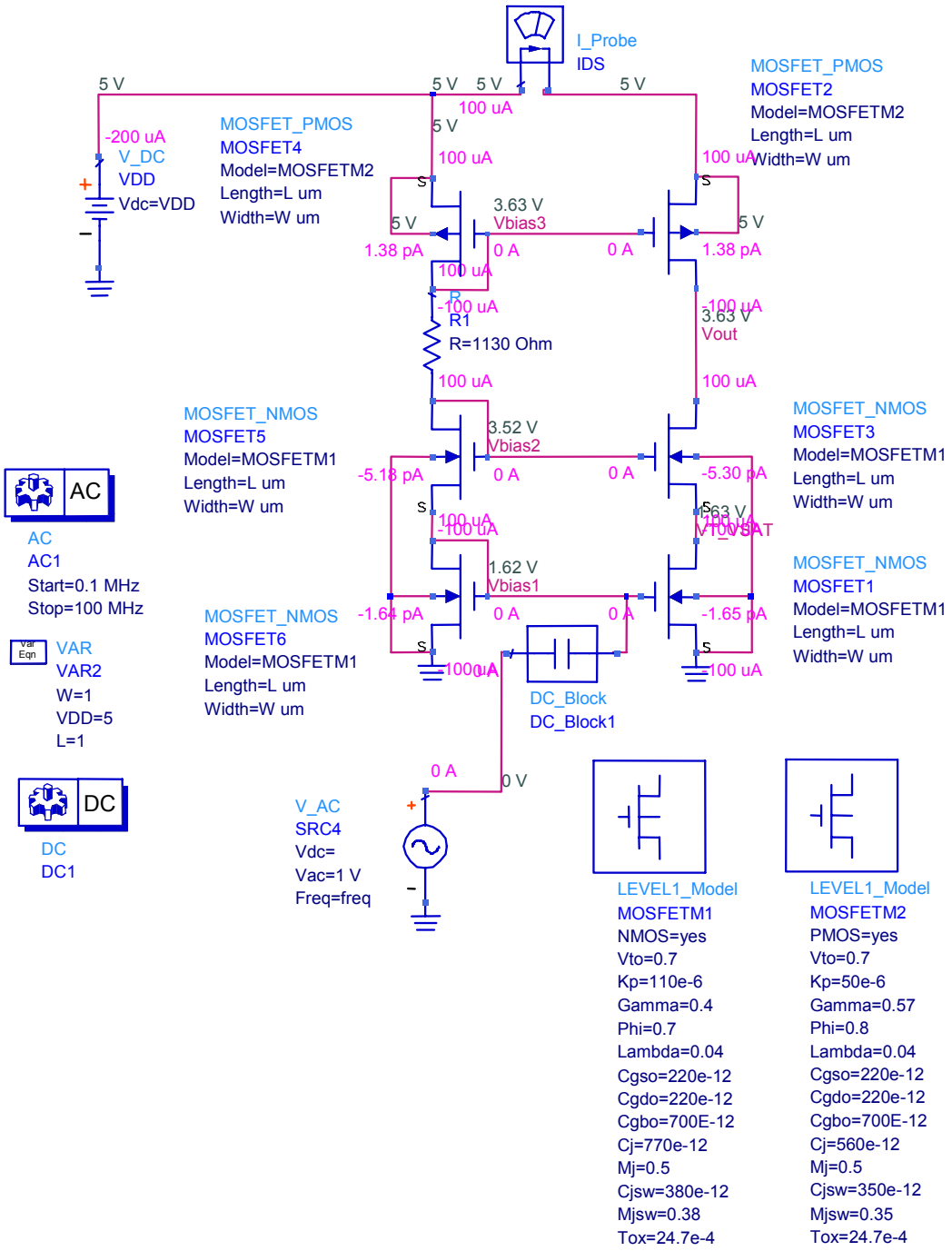
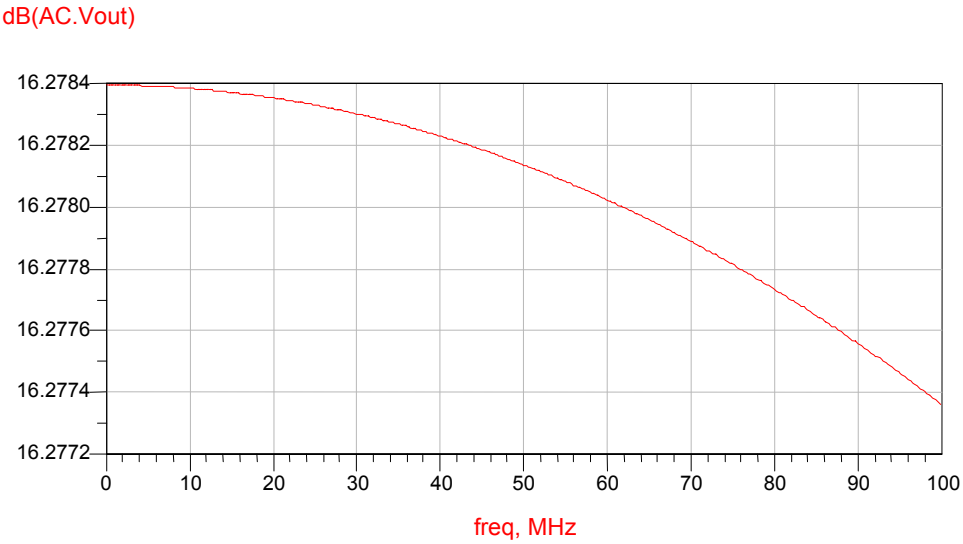


Figure 5 Practical Cascode Amplifier design with added bias

The resulting plot and table of bias voltages is shown in Figure 6.



DC.IDS.i	DC.Vbias1	DC.Vbias2	DC.Vbias3	DC.Vout	DC.VT_VSAT
99.97uA	1.624 V	3.518 V	3.631 V	3.631 V	1.625 V

Figure 6 Resulting plot from the simulation of the circuit shown in Figure 5. Note that VT+VSAT = 1.625V and closely agrees with the 1.65V calculated earlier.

We can obtain more gain from the cascode by adding a further active load as shown in Figure 7. The gain of the stage will now be:-

$$Av = \frac{gm_1}{go_3} \text{ strictly speaking } Av = \frac{gm_1}{go_3 + go_1} \text{ If we cascode the load then}$$

$$Av \approx \left(\frac{gm_1}{go_3}\right)^2 \text{ As } Av = -\sqrt{\frac{2.K_{N1}.W_1}{L_1.I_D.\lambda_3}} \text{ Then the new gain} = -\left(\frac{2.K_{N1}.W_1}{L_1.I_D.\lambda_3}\right)$$

$$Av \approx -\frac{2.K_{N1}.W_1}{L_1.I_D.\lambda_3} = -\frac{2.110E^{-6}.1E^{-6}}{1E^{-6}.100E^{-6}.0.05} = 44 = 32dB$$

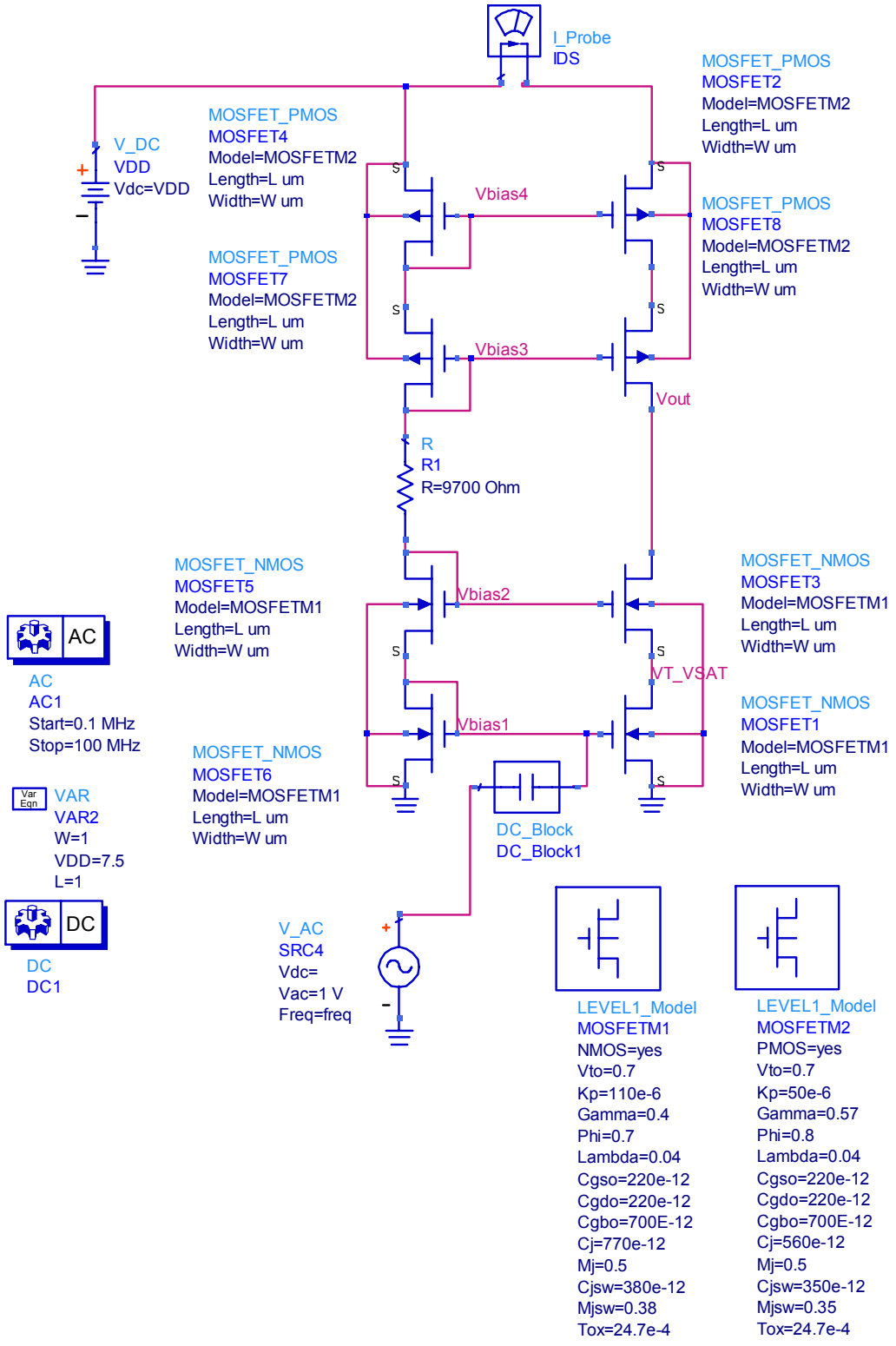
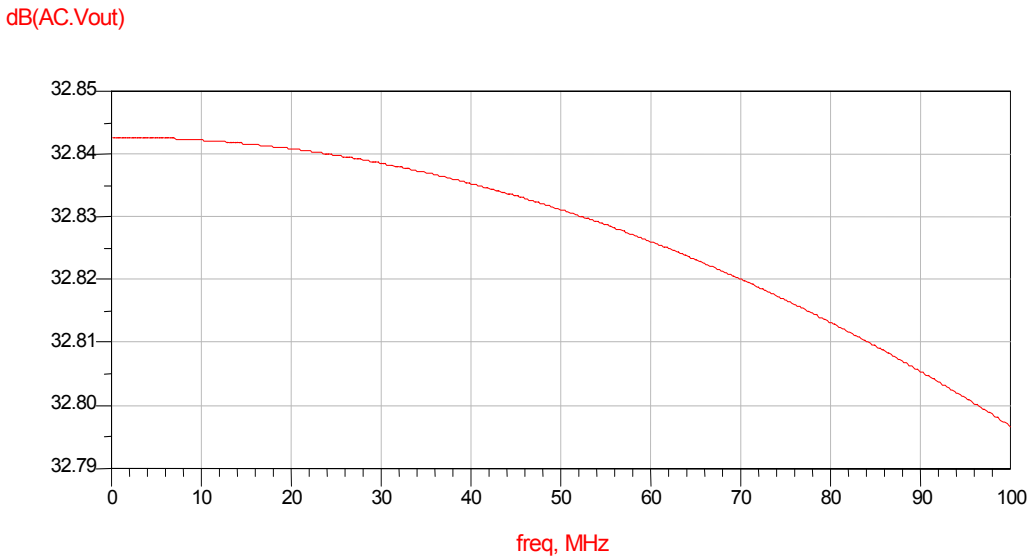


Figure 7 Addition of another active load to increase the gain of the cascode amplifier. Note however that the additional VT+VSAT has meant that to include the bias resistor the supply has been increased to 7.5V.



DC.IDS.i	DC.Vbias1	DC.Vbias2	DC.Vbias3	DC.Vout	DC.VT_VSAT
101.1uA	1.628 V	3.528 V	4.508 V	4.498 V	1.642 V

Figure 8 Increased gain cascode of Figure 7, the gain of 32dB agrees with the calculation performed earlier ie AV ~ $(gm.Ro)^2$.

Note one of the problems using cascode stages in that for each device we use the voltage drop across each device will be VT+VSAT. This equates to approximately 1.65V per device and with 4 devices this will cause a total voltage drop of 6.6V so we can't use our 5V rail !!!. In the example the voltage supply has been increased to 7.5V to allow for the additional device.

This problem of increased voltage rail can be improved by using the folded cascode configuration, where the cascode is split between the active amp and active load and linked by another current load.

Also we can greatly reduce VSAT by increasing the W/L ratio.

The folded cascode is very popular in the design of low voltage Op-Amps and is subject to another tutorial.

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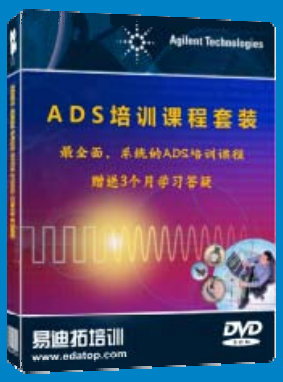

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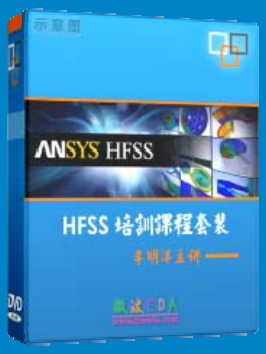

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