**MOS Current Sinks & Mirrors**

As with the BJT circuits in order to realise high voltage gains we require a high RL so that effectively the MOS FET gain will be $-gm r_{ds}$. Realistically if we use an active load using another device we will end up with two r_{ds}'s in parallel giving a voltage gain of:-
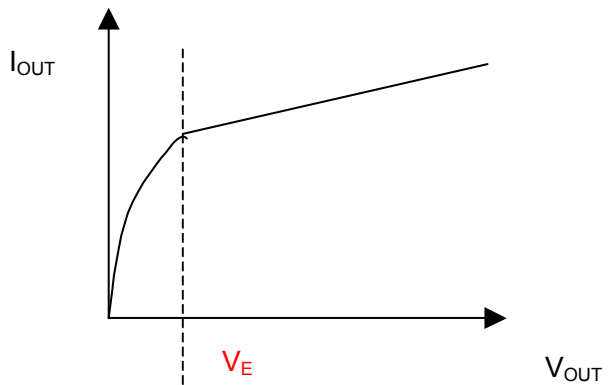
$$A_V = -gm \frac{r_{ds}}{2} \quad \text{Or in terms of conductance where } r_{ds} = \frac{1}{g_O} \quad AV = -gm(2g_O)$$

Current Sink (N-type)

For saturation in constant current region
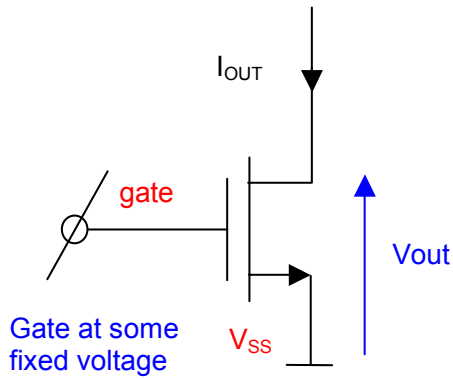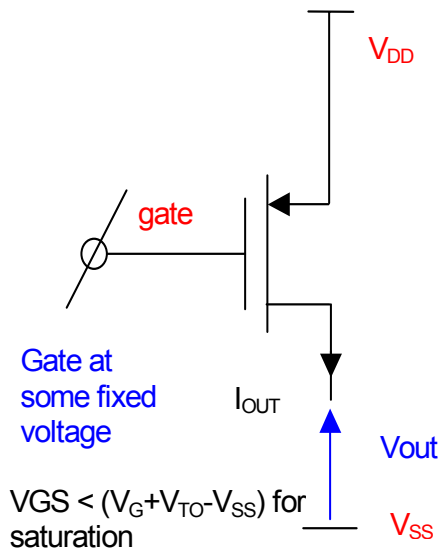

$V_{GS} = (V_G - V_{SS})$

$$V_{DS} > V_E$$
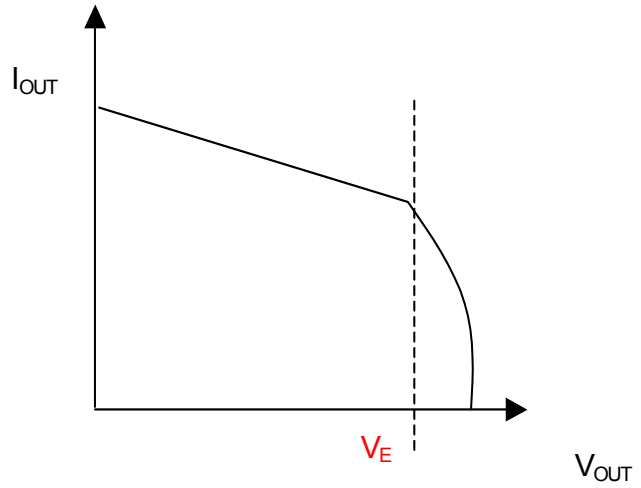
$$V_E = (V_G - V_{SS})$$

$$r_{OUT} = \frac{1}{\lambda . I_{DS}} \approx \frac{1}{g_O} \approx r_{ds}$$

Current Source (P-type)

For saturation in constant current region

Gate at some fixed voltage

$V_{GS} < (V_G + V_{TO} - V_{SS})$ for saturation
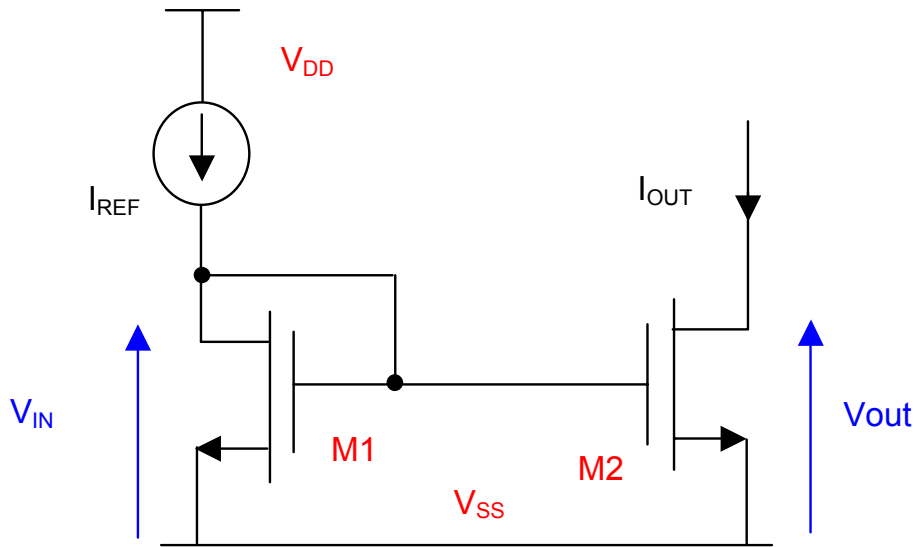
$$V_{DS} > V_E$$

$$V_E = (V_G + V_{TO} - V_{SS})$$

$$r_{OUT} = \frac{1}{\lambda . I_{DS}} \approx \frac{1}{g_O} \approx r_{ds}$$

Simple current Mirror

Advantage is that the circuit is simple with a high output swing but the disadvantage is the low output impedance.

$$V_{IN(MIN)} = V_{DSAT} + V_T$$

$$V_{0MIN} = V_{DSAT}$$

$$R_{IN} \approx \frac{1}{gm_1}$$

$$R_{OUT} = \frac{1}{go_2} = r_{ds2}$$

$$\frac{I_{OUT}}{I_{REF}} = \frac{\left(\dfrac{W_2}{L_2}\right)}{\left(\dfrac{W_1}{L_1}\right)}$$

It is apparent that varying the W/L allows different current sink values for example the next circuit is designed to give a current sinks of 1mA and 2mA. For the design calculation the first MOS device can be considered as a diode – therefore the current set resistor will be (3-0.7)/1mA. The third device has double the width of the first two devices and therefore sinks double the current.

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The circuit below shows the ADS simulation of two current sinks with different W/L ratio's resulting in different sink currents.

DC
DC1
Other=

3 V
−3.85 mA

+ −
0 V

V_DC
SRC1
Vdc=3.0 V

3 V

R
R1
R=2000 Ohm
1.26 V
−868 uA

3 V

R
R2
R=500 Ohm
2.48 V
+1.04 mA
I_Probe
I1

3 V

R
R3
R=500 Ohm
2.03 V
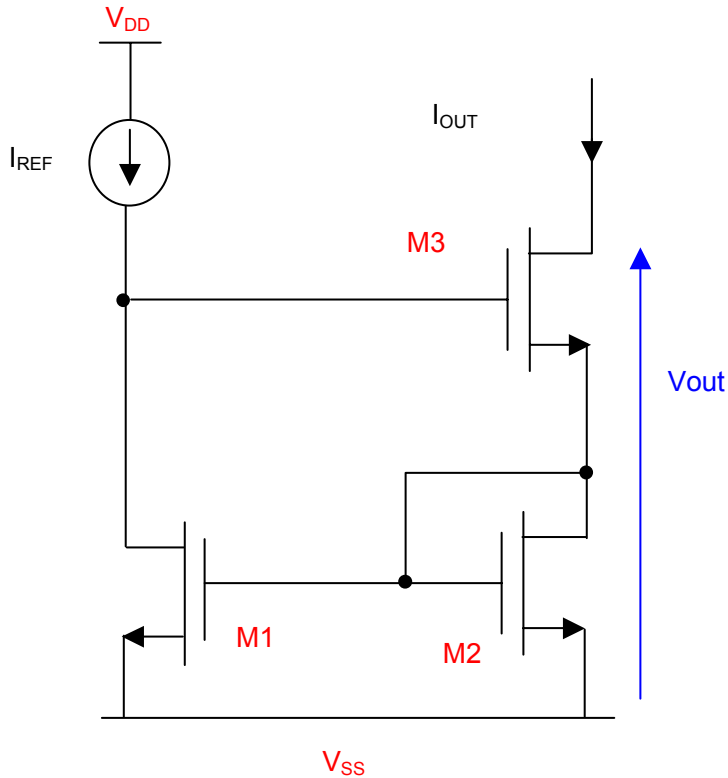+1.95 mA
I_Probe
I2

1.26 V
868 uA

2.48 V
1.04 mA

2.03 V
1.95 mA

−1.28 pA   1.26 V 1.26 V   0 A
0 V   0 A

0 V   1.26 V
−2.50 pA 0 A

0 V
−2.05 pA

0 V
−868 uA
S

0 V
−1.04 mA
S

0 V
−1.95 mA
S

VAR
VAR2
W=100
L=0.5
LAMBDA=0.1/L

LEVEL1_Model
MOSFETM1
NMOS=yes
PMOS=no
Vto=1
Kp=50e-6
Gamma=0.6
Phi=0.8
Lambda=LAMBDA
Rd=
Rs=
Cbd=
Cbs=
Is=
Pb=0.95
Cgso=5e-10
Cgdo=5e-10

Cgbo=
Rsh=
Cj=1e-4
Mj=0.5
Cjsw=5e-10
Mjsw=0.33
Js=
Tox=150e-10
Nsub=
Nss=
Tpg=
Ld=
Uo=
Nlev=
Gdsnoi=1

Kf=
Af=
Fc=
Rg=
Rds=
Tnom=
N=
Tt=
Ffe=
Imax=
AllParams=

MOSFET_NMOS
MOSFET1
Model=MOSFETM1
Length=L um
Width=W um
Ad=
As=
Pd=
Ps=
Nrd=
Nrs=
Mult=2
Region=
Temp=
Mode=nonlinear

MOSFET_NMOS
MOSFET2
Model=MOSFETM1
Length=L um
Width=W um
Ad=
As=
Pd=
Ps=
Nrd=
Nrs=
Mult=2
Region=
Temp=
Mode=nonlinear

MOSFET_NMOS
MOSFET3
Model=MOSFETM1
Length=L um
Width=2*W um
Ad=
As=
Pd=
Ps=
Nrd=
Nrs=
Mult=2
Region=
Temp=
Mode=nonlinear

Wilson Current Mirror

$$V_{OUT(MIN)} = 2V_{DSAT} + V_T$$

$$rout \approx \frac{gm_3}{g_{ds3} \cdot g_{ds1}} \approx gm_3 \cdot (r_{ds3} // r_{ds1})$$

This circuit has high output resistance but suffers from Vds mismatch between M1 & M2.

$$V_{DS1} = 2(V_{DSAT} + V_T) \text{ while } V_{DS2} = V_{DSAT} + V_T$$

If $v_{gs1} = v_{gs2}$ the two drain voltages will be on the same V_{ds} vs I_{ds} curve (for a given v_{gs}) but in different positions. As $1/\lambda$ is finite then the V_{ds} vs I_{ds} curve will not be flat but will have a slope therefore each VDS will have a different value of IDS, so for this current mirror $I_{IN} \neq I_{OUT}$.

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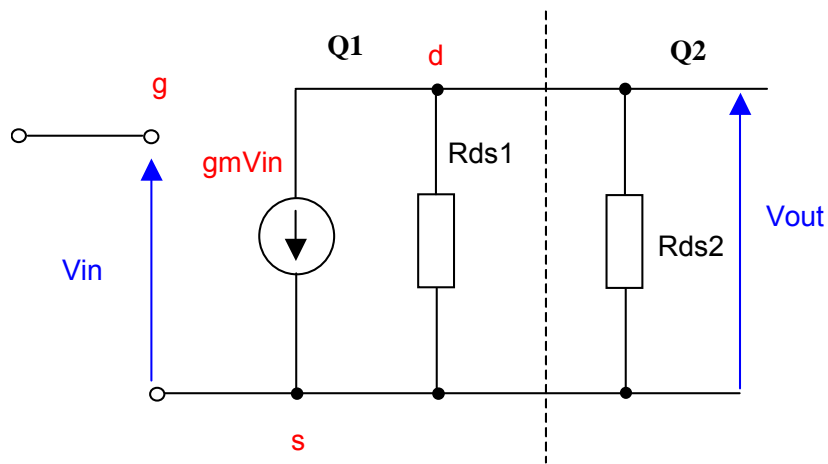
Improved Wilson Current Mirror

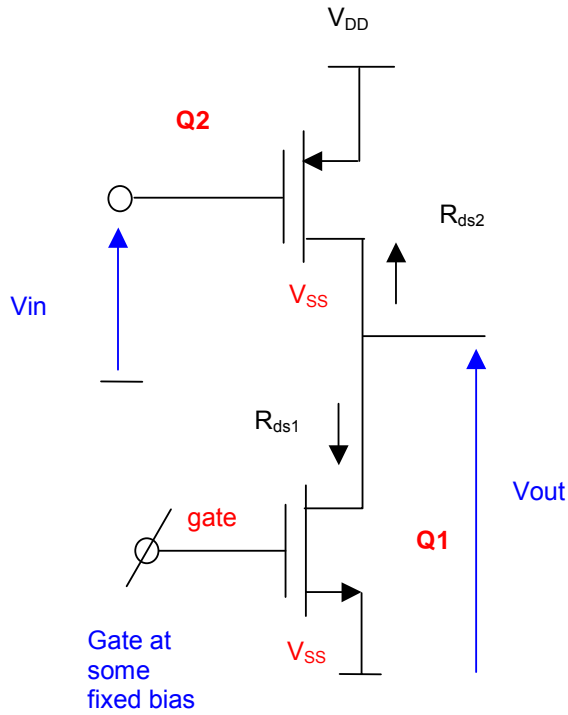We can greatly reduce this mis-match by adding another transistor to the Wilson current mirror, making

$$V_{DS1} = V_{DS2} = V_{DSAT} + V_T$$

The value of r_{out} is the same.
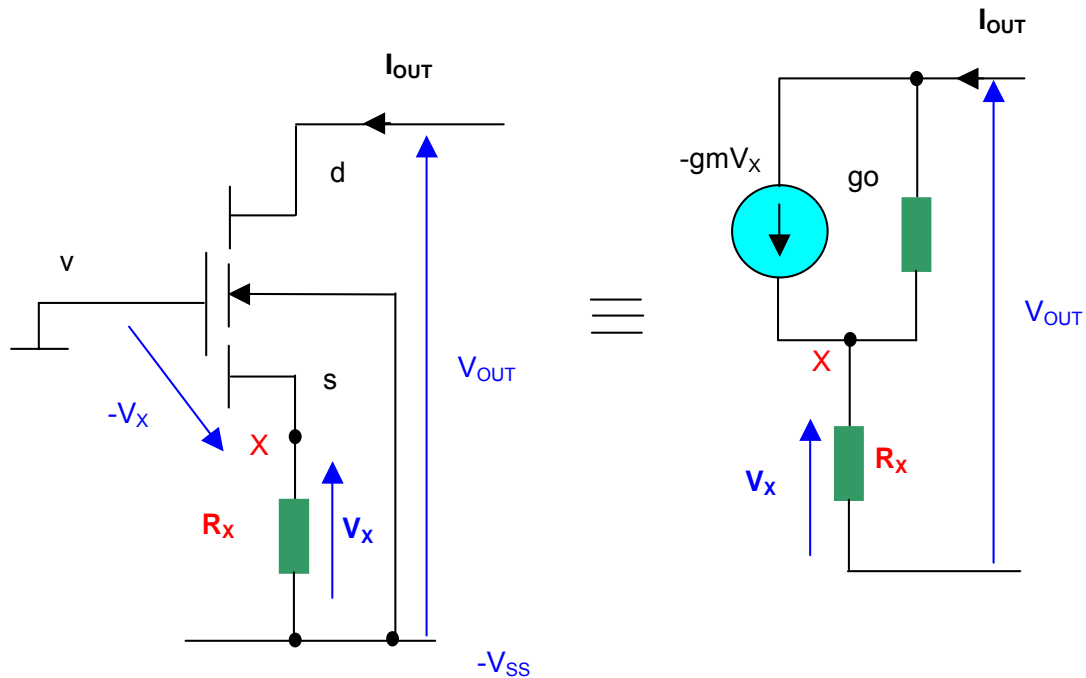
www.rfic.co.uk
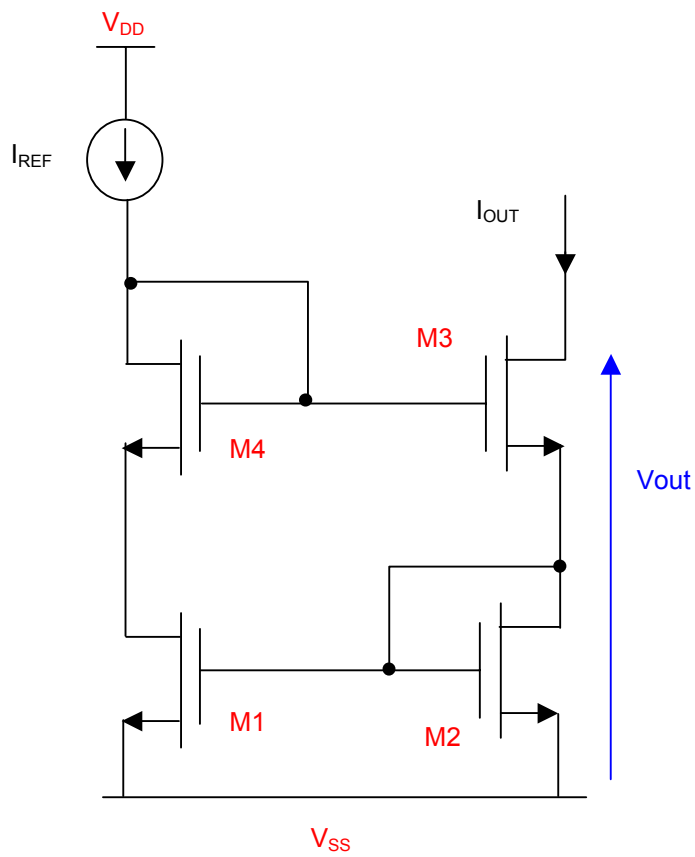
We would like a high resistance load to connect to our amplifier in order to obtain high voltage gain. Adding a current source will do this ie

$$\frac{V_{OUT}}{V_{IN}} = -gm_1(r_{ds1}//r_{ds2}) = -gm_1(go_1 + go_2)$$

The increase of the output resistance is limited to 1/rds but this can be increased by adding a resistor to the source as shown below:

If we assume to start that the source is grounded then the voltage gain A =

$$A = gmR_{ds}$$

$$V_O = A.V_X$$

$$V_O = A.I_O.R_X$$

$$R_{OUT} = \frac{V_O}{I_O} = A.R_X = gmR_{ds}.R_X$$

The next circuit shows the advantages of active loads on the available gain of the circuit. Ideally for high frequency op-amps etc we require the highest gain possible. The circuit runs off a 5V rail and is loaded with a resistor. If we assume a bias current of 10mA and also assume that Vds = 2.5V then this will set the bias load resistor and also the gain.

$$R_{LOAD} = \frac{V_{SS} - V_{DS}}{I_{DS}} = \frac{5 - 2.5}{10x10^{-3}} = 250\Omega$$

A_V then $= -gmR_{LOAD} = -0.027 * 250 = 6.75$ in dB$= 20 * Log(7.75) = 16.6dB$
The circuit was confirmed using an ADS simulation

Include Netlist

spiceInclude
SPICE1
File="tsmc_typical2.net"
NetlistDebugMode=0

DC
DC1
SweepVar=
Start=0
Stop=3
Step=.1
Other=OutVar="MOSFET1.Gm"

AC
AC1
Start=1 MHz
Stop=2000 MHz
Step=

I_Probe
IDS

V_DC
SRC1
Vdc=VDS

R
R2
R=250 Ohm

vout
vout

DC_Block
DC_Block1

V_AC
SRC2
Vac=1 V
Freq=freq

DC_Feed
DC_Feed1

V_DC
SRC3
Vdc=VGS

VAR
VAR1
VGS=1.1
VDS=5

MM9_NMOS
MOSFET1
Model=MODnch3_1
Length=0.5 um
Width=100 um
Ab=
Ls=
Lg=
Temp=
Mult=2
Mode=nonlinear

The gate source voltage (Vgs) is set to 1.1 to give ~ 10mA of drain current. The resulting plot shows the gain agrees with the theory at 16dB.
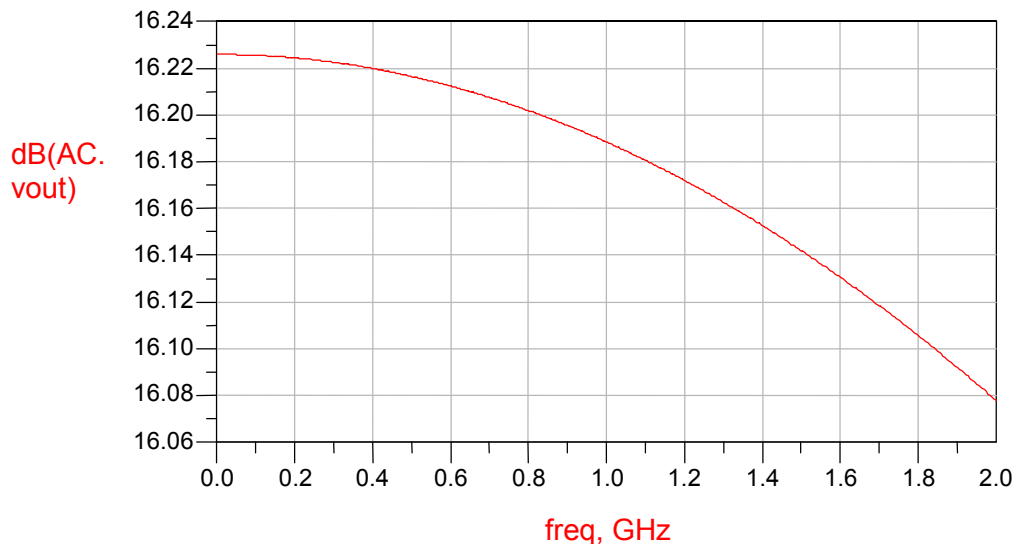
DC.IDS.i	DC.vout	Gm
9.950mA	2.512 V	0.030

If we wanted higher gain – say double to 32dB we would require a larger drain load resistor ie

$$A_{V(dB)} = 20LOG(A_V) \quad \therefore A_V = 10^{\left(\frac{A_{V(dB)}}{20}\right)} \quad A_V = 10^{\left(\frac{32}{20}\right)} = 39.8$$

The load resistor required to give this gain =

$$A_V = gmR_{LOAD} \quad R_{LOAD} = \frac{39.8}{0.027} = 1K47\Omega$$

BUT in order to main the original bias on the device we will now require a larger supply voltage ie

$$V_{LOAD} = R_{LOAD}.I_{DS} = 1470 * 10x10^{-3} = 14.7V$$

$$V_{SS} = V_{LOAD} + V_{DS} = 14.7 + 2.5 \approx 17V$$

Clearly this is inconvenient and is also wasteful in power dissipation. The solution is to use an active load. The following circuit has been modified to include a P-MOS current mirror on the N-MOS device drain to present a high Rds to the N-type device.

I_Probe
IDS

MM9_PMOS
MOSFET5
Model=MODpch3_1
Length=0.5 um
Width=100 um
Ab=
Ls=
Lg=
Temp=
Mult=2
Mode=nonlinear

MM9_PMOS
MOSFET4
Model=MODpch3_1
Length=0.5 um
Width=100 um
Ab=
Ls=
Lg=
Temp=
Mult=2
Mode=nonlinear

vref

vref

vref

S

vout

S

vout

V_DC
SRC1
Vdc=VDS

I_Probe
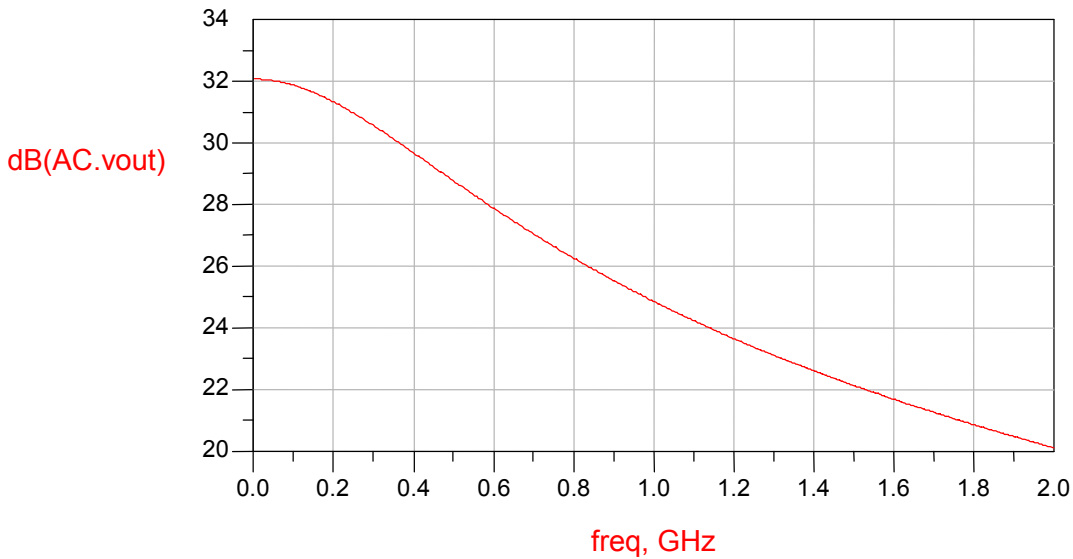Iref

vref

DC_Block
DC_Block1

MM9_NMOS
MOSFET1
Model=MODnch3_1
Length=0.5 um
Width=100 um
Ab=
Ls=
Lg=
Temp=
Mult=2
Mode=nonlinear

Include Netlist

spiceInclude
SPICE1
File="tsmc_typical2.net"
NetlistDebugMode=0

R
R1
R=500 Ohm

V_AC
SRC2
Vac=1 V
Freq=freq

DC_Feed
DC_Feed1

V_DC
SRC3
Vdc=VGS

VAR
VAR1
VGS=.98
VDS=5

DC
DC1
SweepVar=
Start=0
Stop=3
Step=.1
Other=OutVar="MOSFET1.Gm"

AC
AC1
Start=1 MHz
Stop=2000 MHz
Step=

The resulting plot of the CS stage with active P-MOS enhancement load.

DC.IDS.i	DC.vout	Gm	DC.Iref.i	DC.vref
7.522mA	2.534 V	0.027	6.481mA	3.240 V

The only snag with this circuit is that it is difficult to hand calculate the correct bias conditions as they are interactive. Variation in the bias in the current mirror will effect it's resistance and hence the voltage applied to the CS drain and the voltage gain.

The reference P-Type device is acting as a resistor because the gate and source are connected together which, on a P-type enhancement device is below the threshold voltage and the device is working in it's cut-off region.

We will now go through step by step designing the CS amplifier for a 5mA bias.

The first stage is to determine the bias gate voltage required to bias the CS stage with 5mA. To do this we need to simulate the output trace with VDS and obtain the following trace with an applied gate voltage of 0.915V.
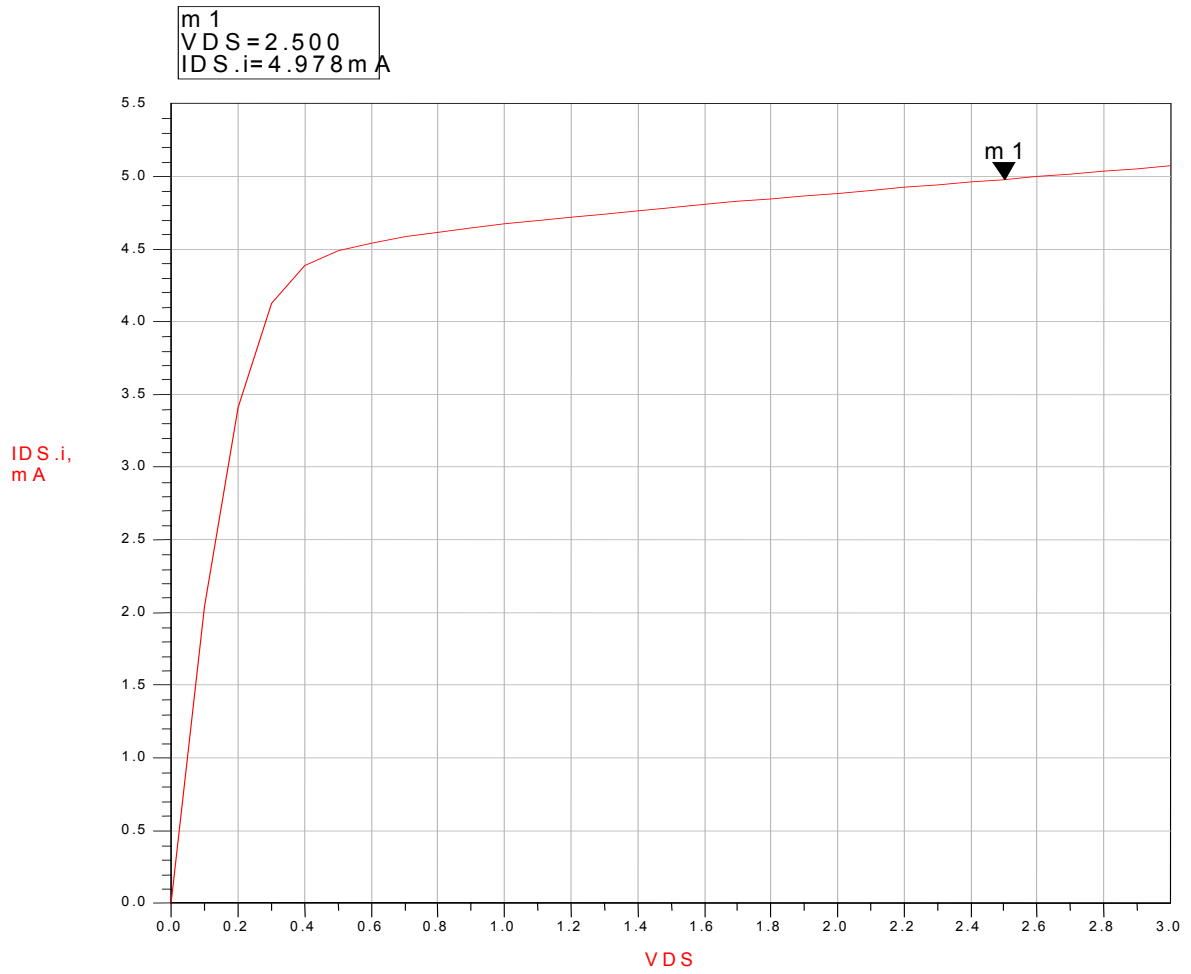
We now need to determine what gate voltage to apply to the P-MOS current source active load also to give 5mA with a VDS of 2.5V.
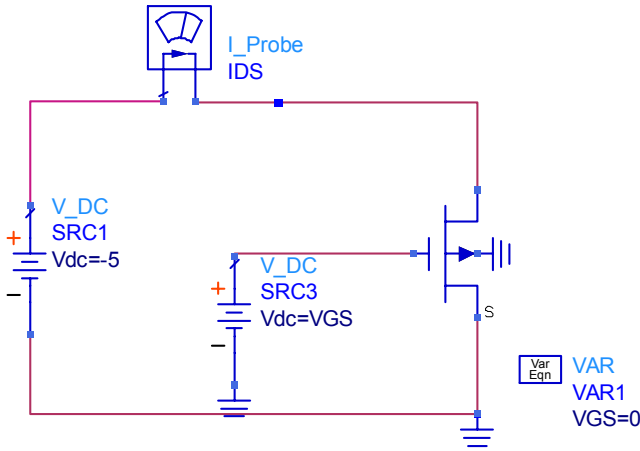
MOSFET_PMOS
MOSFET3
Model=MODpch3_1
Length=0.5 um
Width=100 um
Ad=
As=
Pd=
Ps=
Nrd=
Nrs=
Mult=2
Region=
Temp=
Mode=nonlinear

I_Probe
IDS

V_DC
SRC1
Vdc=-5

V_DC
SRC3
Vdc=VGS

S

Var Eqn   VAR
VAR1
VGS=0

DC

DC
DC1
SweepVar="VGS"
Start=0
Stop=-4
Step=-.1
Other=OutVar="MOSFET1.Gm"

Include Netlist

spiceInclude
SPICE1
File="tsmc_typical2.net"
NetlistDebugMode=0

The resulting plot shows the voltage to get 5mA Ids is –1.6V. Therefore Vref applied to the gate needs to be 5-1.6 = 3.4V.

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m1
VGS=-1.600
plot_vs(IDS.i, VGS)=-0.005

Finally we need to simulate the P-MOS device with gate-source 0V and a load resistor connected ie

I_Probe
IDS

V_DC
SRC1
Vdc=5

VAR
VAR1
LOAD=0
VDS=3.3   v r e f

MOSFET_PMOS
MOSFET3
Model=MODpch3_1
Length=0.5 um
Width=100 um
Ad=
As=
Pd=
Ps=
Nrd=
Nrs=
Mult=2
Region=
Temp=
Mode=nonlinear

S
v r e f

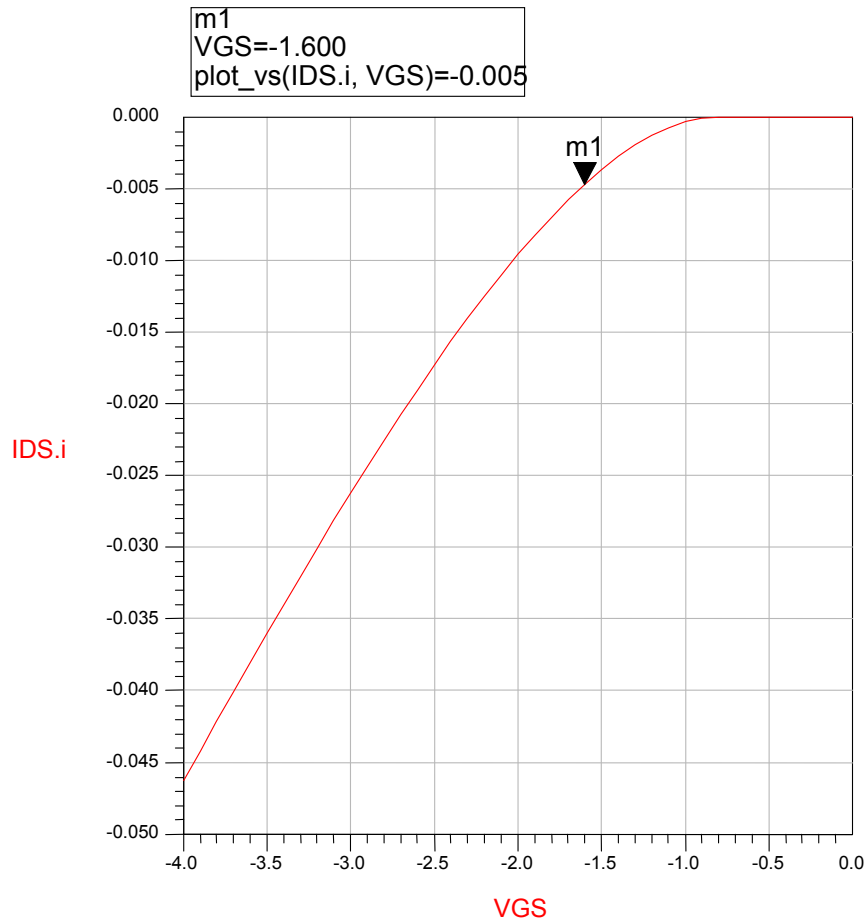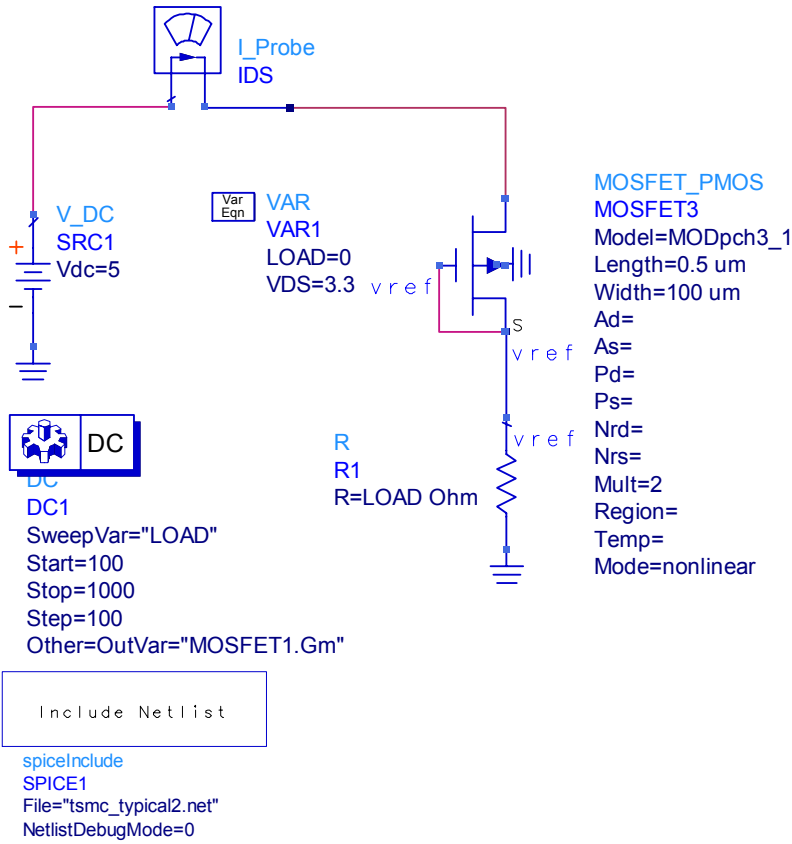v r e f

DC
DC1
SweepVar="LOAD"
Start=100
Stop=1000
Step=100
Other=OutVar="MOSFET1.Gm"

R
R1
R=LOAD Ohm

Include Netlist

spiceInclude
SPICE1
File="tsmc_typical2.net"
NetlistDebugMode=0

Resulting simulation result.

LOAD	vref
100.000	2.174 V
200.000	2.677 V
300.000	2.944 V
400.000	3.117 V
500.000	3.240 V
600.000	3.335 V
700.000	3.410 V
800.000	3.472 V
900.000	3.523 V
1000.000	3.567 V
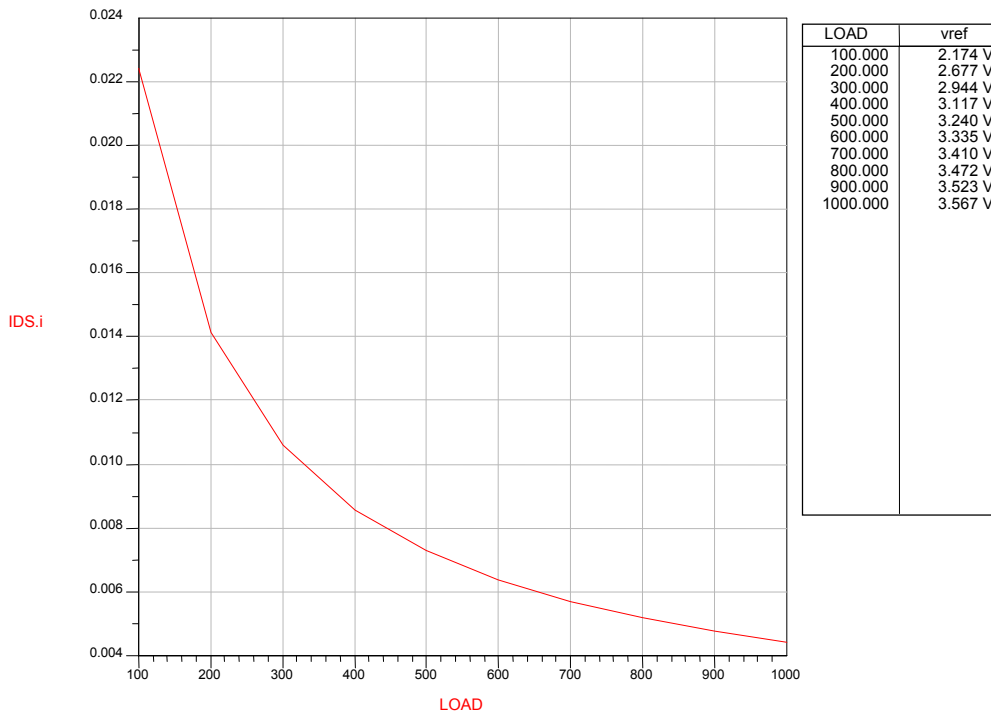
We can see that to achieve a gate voltage of 3.4V we set the load resistor to 700ohms

Putting all these blocks together we can simulate the complete amplifier now set with a bias current through the CS stage of 5mA.

I_Probe
IDS

MM9_PMOS
MOSFET5
Model=MODpch3_1
Length=0.5 um
Width=100 um
Ab=
Ls=
Lg=
Temp=
Mult=2
Mode=nonlinear

vref

vref

vref

V_DC
SRC1
Vdc=VDS

I_Probe
Iref

vref

R
R1
R=700 Ohm

MM9_PMOS
MOSFET4
Model=MODpch3_1
Length=0.5 um
Width=100 um
Ab=
Ls=
Lg=
Temp=
Mult=2
Mode=nonlinear

vref

S

vout

vout

S

DC_Block
DC_Block1

V_AC
SRC2
Vac=1 V
Freq=freq

DC_Feed
DC_Feed1

MM9_NMOS
MOSFET1
Model=MODnch3_1
Length=0.5 um
Width=100 um
Ab=
Ls=
Lg=
Temp=
Mult=2
Mode=nonlinear

Include Netlist

spiceInclude
SPICE1
File="tsmc_typical2.net"
NetlistDebugMode=0

DC
DC1
SweepVar=
Start=0
Stop=3
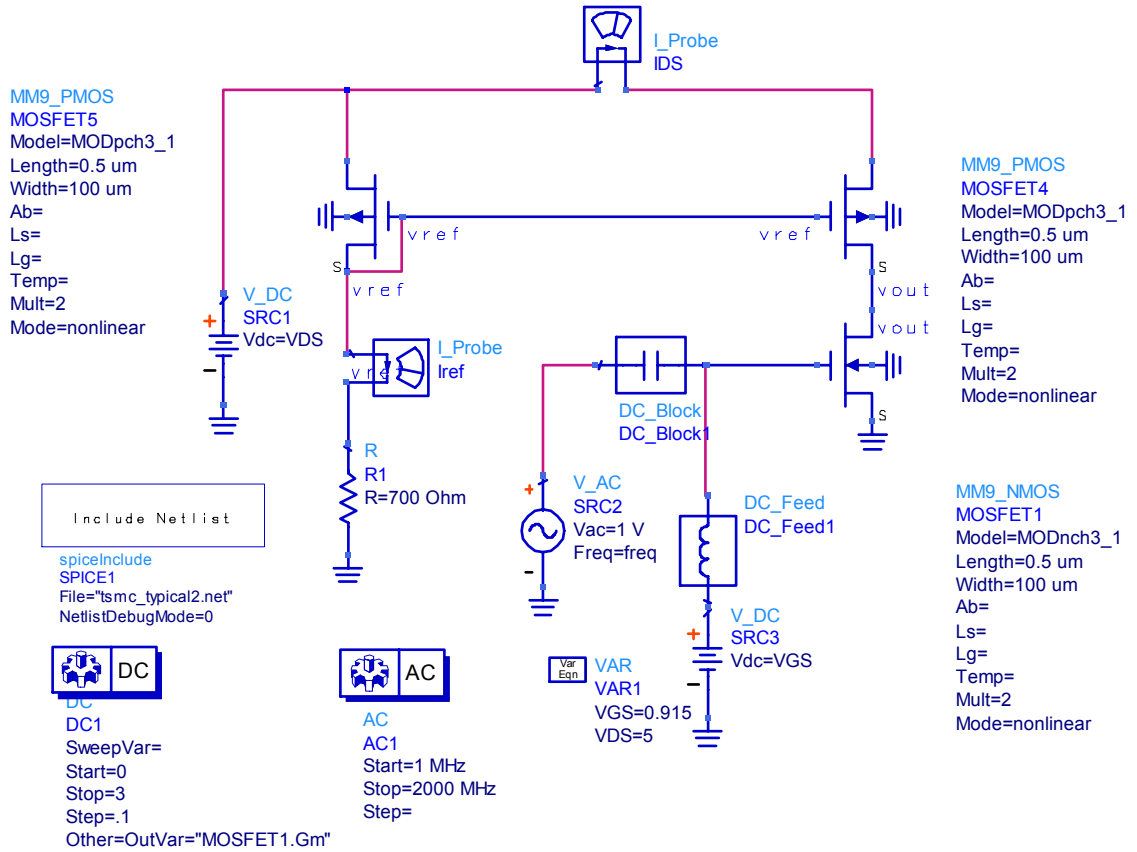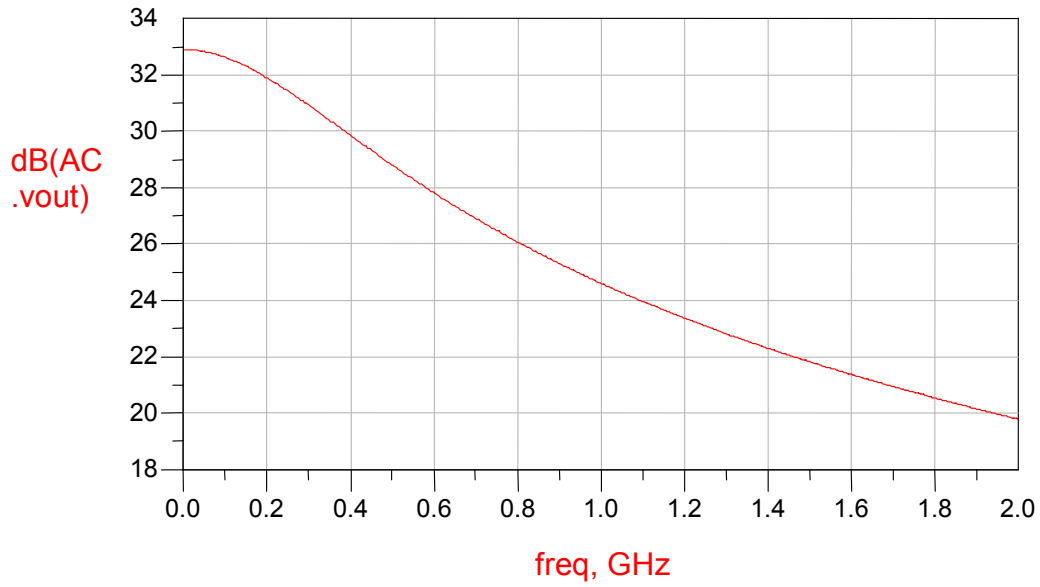Step=.1
Other=OutVar="MOSFET1.Gm"

AC
AC1
Start=1 MHz
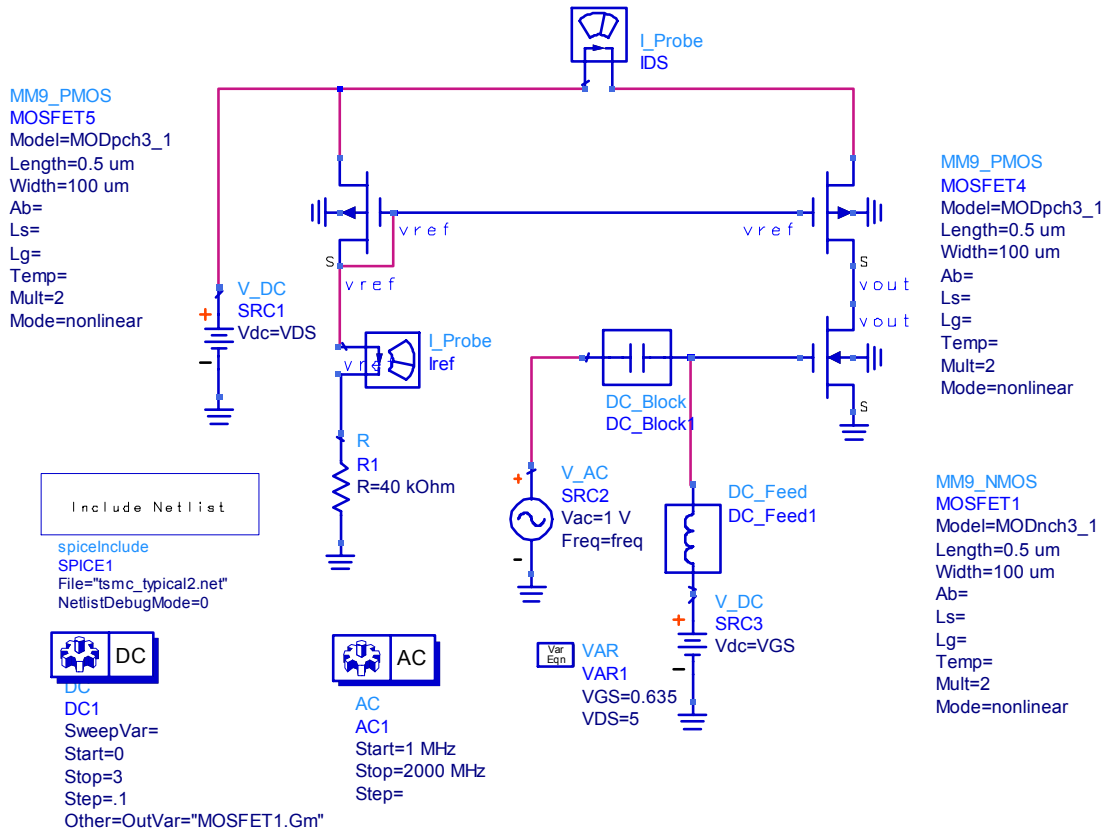Stop=2000 MHz
Step=

VAR
VAR1
VGS=0.915
VDS=5

V_DC
SRC3
Vdc=VGS

Resulting final plot of the amplifier voltage gain and bias points showing the Vref at 3.4V and the VDS on the CS stage at 2.5V as required.

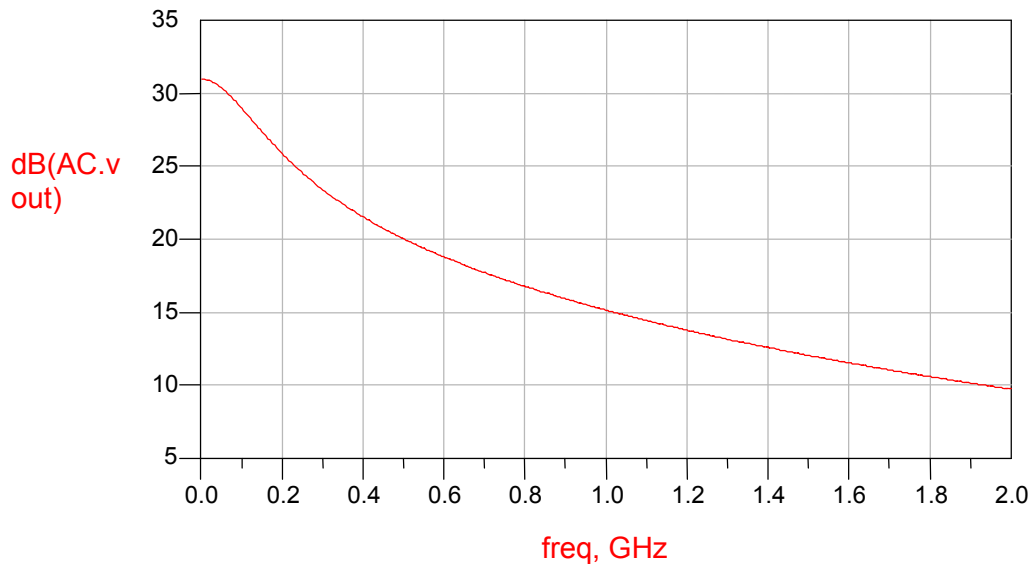www.rfic.co.uk

DC.IDS.i	DC.vout	Gm	DC.Iref.i	DC.vref
5.937mA	2.512 V	0.025	4.872mA	3.410 V

Finally the circuit has been re-designed for a bias current of 1mA – NOTE the very large Load resistor required:

MM9_PMOS
MOSFET5
Model=MODpch3_1
Length=0.5 um
Width=100 um
Ab=
Ls=
Lg=
Temp=
Mult=2
Mode=nonlinear

I_Probe
IDS

V_DC
SRC1
Vdc=VDS

I_Probe
Iref

R
R1
R=40 kOhm

DC_Block
DC_Block1

V_AC
SRC2
Vac=1 V
Freq=freq

DC_Feed
DC_Feed1

V_DC
SRC3
Vdc=VGS

MM9_PMOS
MOSFET4
Model=MODpch3_1
Length=0.5 um
Width=100 um
Ab=
Ls=
Lg=
Temp=
Mult=2
Mode=nonlinear

MM9_NMOS
MOSFET1
Model=MODnch3_1
Length=0.5 um
Width=100 um
Ab=
Ls=
Lg=
Temp=
Mult=2
Mode=nonlinear

Include Netlist
spiceInclude
SPICE1
File="tsmc_typical2.net"
NetlistDebugMode=0

DC
DC1
SweepVar=
Start=0
Stop=3
Step=.1
Other=OutVar="MOSFET1.Gm"

AC
AC1
Start=1 MHz
Stop=2000 MHz
Step=

VAR
VAR1
VGS=0.635
VDS=5

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dB(AC.vout)

DC.IDS.i	DC.vout	Gm	DC.Iref.i	DC.vref
1.085mA	2.550 V	0.007	104.5uA	4.180 V

In Summary the use of an active P-MOS load allows for a high gain circuit by presenting a high load resistor to the CS stage ie Rds in parallel with the CS stage Rds, but sourcing the required current. A resistor can be used, but for high gains a large resistor is required resulting in a large supply rail if using high bias currents.

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课程网址：http://www.edatop.com/peixun/rfe/110.html

ADS 学习培训课程套装

该套装是迄今国内最全面、最权威的 ADS 培训教程，共包含 10 门 ADS 学习培训课程。课程是由具有多年 ADS 使用经验的微波射频与通信系统设计领域资深专家讲解，并多结合设计实例，由浅入深、详细而又全面地讲解了 ADS 在微波射频电路设计、通信系统设计和电磁仿真设计方面的内容。能让您在最短的时间内学会使用 ADS，迅速提升个人技术能力，把 ADS 真正应用到实际研发工作中去，成为 ADS 设计专家…

课程网址：　http://www.edatop.com/peixun/ads/13.html

HFSS 学习培训课程套装

该套课程套装包含了本站全部 HFSS 培训课程，是迄今国内最全面、最专业的 HFSS 培训教程套装，可以帮助您从零开始，全面深入学习 HFSS 的各项功能和在多个方面的工程应用。购买套装，更可超值赠送 3 个月免费学习答疑，随时解答您学习过程中遇到的棘手问题，让您的 HFSS 学习更加轻松顺畅…

课程网址：http://www.edatop.com/peixun/hfss/11.html

CST 学习培训课程套装

该培训套装由易迪拓培训联合微波 EDA 网共同推出，是最全面、系统、专业的 CST 微波工作室培训课程套装，所有课程都由经验丰富的专家授课，视频教学，可以帮助您从零开始，全面系统地学习 CST 微波工作的各项功能及其在微波射频、天线设计等领域的设计应用。且购买该套装，还可超值赠送 3 个月免费学习答疑…

课程网址：http://www.edatop.com/peixun/cst/24.html

HFSS 天线设计培训课程套装

套装包含 6 门视频课程和 1 本图书，课程从基础讲起，内容由浅入深，理论介绍和实际操作讲解相结合，全面系统的讲解了 HFSS 天线设计的全过程。是国内最全面、最专业的 HFSS 天线设计课程，可以帮助您快速学习掌握如何使用 HFSS 设计天线，让天线设计不再难…

课程网址：http://www.edatop.com/peixun/hfss/122.html

13.56MHz NFC/RFID 线圈天线设计培训课程套装

套装包含 4 门视频培训课程，培训将 13.56MHz 线圈天线设计原理和仿真设计实践相结合,全面系统地讲解了 13.56MHz 线圈天线的工作原理、设计方法、设计考量以及使用 HFSS 和 CST 仿真分析线圈天线的具体操作，同时还介绍了 13.56MHz 线圈天线匹配电路的设计和调试。通过该套课程的学习，可以帮助您快速学习掌握 13.56MHz 线圈天线及其匹配电路的原理、设计和调试…

详情浏览：http://www.edatop.com/peixun/antenna/116.html

我们的课程优势：

※ 成立于 2004 年，10 多年丰富的行业经验，

※ 一直致力并专注于微波射频和天线设计工程师的培养，更了解该行业对人才的要求

※ 经验丰富的一线资深工程师讲授，结合实际工程案例，直观、实用、易学

联系我们：

※ 易迪拓培训官网：http://www.edatop.com

※ 微波 EDA 网：http://www.mweda.com

※ 官方淘宝店：http://shop36920890.taobao.com