



BIOGRAPHICAL SKETCH

Stephen Long received his BS degree in Engineering Physics from UC Berkeley and MS and PhD in Electrical Engineering from Cornell University. He has been a professor of electrical and computer engineering at UC Santa Barbara since 1981. The central theme of his current research projects is rather practical: use unconventional digital and analog circuits, high performance devices and fabrication technologies to address significant problems in high speed electronics such as low power IC interconnections, very high speed digital ICs, and microwave analog integrated circuits for RF communications. He teaches classes on communication electronics and high speed digital IC design.

Prior to joining UCSB, from 1974 to 1977 he was a Senior Engineer at Varian Associates, Palo Alto, CA. From 1978 to 1981 he was employed by Rockwell International Science Center, Thousand Oaks, CA as a member of the technical staff.

Dr. Long received the IEEE Microwave Applications Award in 1978 for development of InP millimeter wave devices. In 1988 he was a research visitor at GEC Hirst Research Centre, U.K. In 1994 he was a Fulbright research visitor at the Signal Processing Laboratory, Tampere University of Technology, Finland and a visiting professor at the Electromagnetics Institute, Technical University of Denmark. He is a senior member of the IEEE and a member of the American Scientific Affiliation.



The mixer DesignGuide is intended to enhance productivity of RF designers by providing an extensive collection of analysis tools that can be easily loaded into your project from a pulldown menu. Each pair of these analysis network and displays, which could take days to set up and verify, can be easily adapted for your mixer circuit simulation requirements.



A transmit mixer application is selected to illustrate a design procedure that is enabled by the Mixer DesignGuide. The input baseband or IF signal is centered at 200 MHz. The output is at 1.8 GHz. We will assume that the mixer is intended for a base station power amplifier application.

The mixer will use 0.35 μ m MOSFETs with a default device model parameter set. Of course, you will need to substitute your own verified MOSFET model parameters for the default set. Otherwise, there would be no hope of any correspondence between simulation and measurement for the mixer characteristics that are more sensitive to model nonlinearities. This would especially be true for intermodulation simulations and noise.



There are many different performance specifications for mixers. Some are of interest for receive applications where the input signal level is not under the control of the designer. In this case, the maximum linearity under large signal drive conditions is often very critical. Noise figure may be of secondary concern.

For the transmit application used here as an illustration, the designer has control of the signal level. Then, the design strategy shifts to trading off noise and IMD behavior in order to achieve the largest useable dynamic range.

As an extra illustration, after the intrinsic mixer performance is evaluated, the design will be modified to improve conversion gain and image rejection by tuning the mixer output. Secondly, a differential-to-single ended converter will be added to interface to an off-chip bandpass filter.



The analysis tools are accessible by the DesignGuide pulldown menu. Select Mixer DesignGuide, then scroll through the list to find the relevant analysis. Then, the schematic and display panels will be loaded into your project.



The mixer under test is constructed as an ADS subnetwork. The mixer itself can be replaced with or modified to become your own design. Select the mixer, push down into the subnetwork, and replace the circuit with your own design. If you use the Diff_MixerUnderTest as your subnetwork, and insert your design, the design is automatically inserted into all of the analysis circuit templates. Or, you can save your design under a different name, select it using the component library icon on the toolbar, and replace the default mixer with your own.

You can declare any of the circuit parameters to be accessible outside of the subnetwork by using the File > Design Parameters panel. In this example, VDD, RD (drain resistance), WCSP (current source control width), W1 and W2 (transconductance and switch MOSFET widths), and source degeneration resistance (RS) and inductance (LS) are all available for a parameter sweep.



You then will configure the simulation controller, HB in this example, with the appropriate parameters.

Order[1] number of LO harmonics - should be large for switching mixers

Order[2] number of harmonics at the mixer signal input - small if input amplitude is small; larger if you are simulating the mixer near the 1 dB compression point

MaxOrder maximum sum of the LO and Input harmonics considered in the solution. Generally, you would use the sum: Order[1]+Order[2]

SweepVar: This is the swept parameter, in this example the LO power. Set the range and step size used for the simulation.

Note that the data file size will increase with the order and with the number of sweep steps.



We will utilize the DesignGuide mixer library as a starting point for the design exercise. This is a schematic of a MOSFET version of the Gilbert active doublebalanced mixer. The lower FET diff pair serves as a transconductance amplifier. The upper FETs provide a fully balanced, phase-reversing current switch. A DC bias generator is included (not shown) which will keep the MOSFETs in their active region.

The large signal handling capability of the mixer will depend mainly upon the linearity of the transconductance amplifier, and is measured by determining the maximum input voltage (or power in some cases) that causes a 1 dB compression in the conversion gain. The maximum linear input voltage range can be increased by increasing the source degeneration resistors, Rs. While source inductance can also provide beneficial degeneration, in this case, we have a very low input IF frequency, 200 MHz. The inductance values required would be too large for RFIC implementation, thus we are stuck with the resistors (they will add noise). The load resistors could also cause gain compression if the voltage swing at the drains is large enough to cause the output to clip under large signal drive conditions.

The double-balanced design rejects IF and LO feedthrough to the output if the output is taken differentially. This is because the LO component in the output is a common mode signal while the RF output is differential.

For a more complete explanation of how the Gilbert cell mixer operates, refer to the reference list at the end of this presentation.

| The example design sequer mixer. Our goal is to increa and matching are not as cr | nce is suited for an upconversion ise dynamic range. Conversion ga itical. | iin |
|---|--|-----|
| 1. LO amplitude: Conversion | n gain, V _{in} at 1 dB gain compressio | n |
| 2. Gain Compression: source | e resistance Rs, drain resistance, | Rd |
| 3. Noise figure: Rs, I_bias | | |
| 4. Dynamic Range vs. Input | Voltage | |
| 5. Spectral spreading and A | CPR with digital modulation | |
| | | |
| | | |

A mixer that is to be used for base station transmit applications requires high linearity and low noise so that the least amount of spurious power is spread into the adjacent channel. We will optimize our mixer in the following sequence:

1. LO amplitude. You want to make sure the mixer commutating switch is fully activated. Excess distortion can be produced with a weakly conducting or slowly activated switch. Use the conversion transducer gain and 1 dB gain compression input level to determine when the LO voltage is sufficient.

2. Evaluate the influence of source and drain resistance on the 1 dB compression level. This will give insight into the principal mechanisms that limit linearity.

3. The added noise of the mixer will affect the minimum signal level and thus limit dynamic range. There will be a tradeoff between noise, gain, and gain compression.

4. The two-tone 3rd order intermodulation distortion power and the noise figure determine the mixer dynamic range vs. input voltage. Since for transmit applications you have complete control over your input voltage, find the optimum dynamic range - the mixer's "sweet spot" for best performance. Or, alternatively, if you have a fixed signal level, design the mixer to provide the best dynamic range at that signal level.

5. Finally, test the mixer under more realistic signal excitation - using a CDMA source, for example, to emulate a multicarrier environment. This is a more severe test than the two-tone IMD one, and is much more time consuming to simulate since a large number of symbols must be used for accurate results.



Once the basic resistively loaded Gilbert cell mixer is characterized, two modifications will be employed to improve performance. First, the mixer drain nodes will be tuned with inductors and a capacitor for resonance at the output frequency. This improves conversion gain if inductors with reasonable Qu can be fabricated. It also decreases the amplitude of the undesired output image because of its bandpass transfer function. The image must be removed anyway, and it's presence can only degrade the distortion of the output stage by increasing the peak voltage present at its input.

The output of the mixer will need to be filtered off-chip with a SAW filter before further amplification, so a single ended output is more efficient. The last stage is added to perform a differential to single ended conversion. It must have good common mode rejection to suppress LO feedthrough and good linearity so that it doesn't degrade dynamic range.



The first step is to determine a suitable LO voltage that provides a reasonable compromise between conversion gain and LO power and at the same time does not limit the 1 dB gain compression input voltage. The MOSFETs forming the commutating switch (upper level) must be driven hard enough to present a low series resistance to the load. Most of the mixer analysis schematic and display templates available in the DesignGuide library include an LO power sweep capability. Use the menu as shown to select a conversion gain simulation as a function of LO power. Also, a NdB Gain Compression analysis can be used to evaluate the dependence of gain compression on LO drive.

From these simulations, we see that the input power at which gain compresses by 1 dB (P1dB) is not a strong function of LO voltage, but conversion gain is somewhat dependent. The more gate voltage applied to the upper tier of MOSFETs, the lower their series resistance relative to the drain resistance and thus the higher the conversion gain. We also can see that there is a conversion loss which gets worse at the higher output RF frequency of 1.8 GHz, but we can improve on this later by tuning the RF output of the mixer.



Gain compression is evaluated using the N-dB Gain Compression Point analysis schematic. The 1dB gain compression input power and input voltage are found for swept parameters. In this case, the influence of R_S and R_D on V_{1dB} was determined. The R_S sweep used $R_D = 100\Omega$. The R_D sweep set $R_S = 30\Omega$. Conversion gain is measured at the 1 dB compressed level. Alternatively, a two-dimensional sweep could also be set up using an extra Parameter Sweep controller.

In an RFIC mixer where the input might not be matched to a source impedance, the input voltage is a more important metric of gain compression than the input available power (P1dB) since available power assumes a conjugately matched source and load. Also, in a multi-signal environment, the peak input voltage can be quite large at the instant in time when all signals add in phase. It is this peak voltage that determines the distortion limits of the mixer. For example, the two-tone IMD simulations will predict a 1 dB compression power 6 dB lower than single tone simulations because the peak voltage will be twice as high for the same power per tone.

It is also interesting to note that the conversion power gain depends inversely on R_D . In the simulation, the external load resistance was set to 2 R_D so that the output power (power absorbed in the load) is also the available output power,

 $P_{out} = V_{out}^2/4R_D$. The voltage gain would be expected to follow R_D/R_S but increases less rapidly than anticipated, probably due to the output RC time constant bandwidth limitations.



We can simulate the mixer single-sideband noise figure as a function of DC bias current through the Gilbert cell (mixer core). The DC current is varied by sweeping the width of the PMOS current source Wcsp and the mixer current mirror width Wcs using a parameter sweep.

SSB noise figure is appropriate because only one input frequency is applied to the mixer, but wideband noise at the image frequency and from LO harmonics is included in the signal to noise calculation. We find that the NF is reduced with increasing I_bias, but reaches a point of diminishing returns. Thus, a width of 50 μ m was selected as a compromise between power and noise.

The device widths in this mixer have been selected to minimize noise [3].



We also find a strong dependence of SSB NF on the source resistance. This is expected because the thermal noise contributed by the resistor is directly in the input voltage loop of the differential pair. Thus, we will need to trade off V1dB and noise figure to obtain the largest dynamic range of the mixer.

The dynamic range at low input signal power levels will be limited by the carrier to noise ratio. The noise power for a minimum detectable signal (S/N = 1) depends on both NF and the noise bandwidth. This bandwidth will normally be set by an external SAW filter between the mixer and the driver amplifier. The filter is also required to reject the output difference ($F_{LO} - F_{IN}$) image frequency at 1.4 GHz.

The conversion gain (a loss in this case) may also increase the noise figure because the drain resistor thermal noise is input referred through the gain. Thus, we will also want to investigate a tuned output to eliminate some of this noise.



You can also perform a two parameter sweep by selecting a second Parameter Sweep controller. In this example, the variation in noise figure with RS and RD that was displayed in tables on the previous slide can now be plotted as constant NF contours using the contour function in the function library.



You can do the same thing with the conversion gain data.



At higher input signal levels, the dynamic range of the mixer is limited by the distortion. The third-order intermodulation distortion products are the most damaging because they show up in-band and cannot be rejected by the filter.

A two-tone third-order IMD simulation with an RF power sweep can be used to display the carrier-to-IMD power ratio. The IMD power present in the output will increase at 3 times the rate of increase of input power. Thus, the difference between output power and IMD power shrinks with increasing input.

At low input signal levels, the noise floor, set by the mixer noise figure and the noise bandwidth of the mixer-bandpass filter-amplifier cascade, will set a lower limit to the output power from the mixer. The dotted lines above show this noise floor in red. The blue dotted line represents the mixer output power vs. RF input power at this lower input regime. It has a slope of 1. You can see that the difference between output power and noise floor shrinks as the power decreases.

The maximum dynamic range is found at the inflection point.



Here, we have taken outputs from two simulations: IMD RF power sweep and the SSB NF. The dynamic range is controlled by the least of these two conditions:

| DR = Pout (de | sm) – MDS (aBr | n) | for low inp (noise lim | ited) |
|---------------|----------------|-----|---------------------------|--------------|
| DR = Pout (dE | Bm) – PIMD (dB | m) | for higher | input levels |
| | | | (distortior | n limited) |
| Rs | DR (dB) | Vir | ו (V) | NF (dB) |
| | | (di | fferential) | |
| 10 | 57.7 | 0.0 | 17 | 6.5 |
| 20 | 57.3 | 0.0 | 25 | 8 |
| 30 | 56.4 | 0.0 | 31 | 9.2 |
| 40 | 56.0 | 0.0 | 39 | 10.3 |

The dynamic range peak will depend on the noise bandwidth. For narrower bandwidths, the noise floor will drop and the peak DR will increase but shift to lower differential input voltage. The 30 MHz noise bandwidth was chosen because of the base station application. The transmitter should be capable of covering an entire frequency band.



The low conversion gain of the resistively loaded mixer will cause higher noise due to the drain resistors. By resonating the output at 1.8 GHz, the conversion gain is increased and the gain at the image (1.4 GHz) is reduced. The comparison between the resistive loaded case and the tuned case shows an increase in conversion gain by about 3.5 dB.

You can perform an RF frequency sweep to find the resonant frequency. From that, you can calculate how much capacitance is contributed by the drain-to-substrate junction and absorb it into the resonator.

An unloaded Q = 5 is assumed for the inductor.



On chip inductor Q is limited by metal losses and substrate conduction in bulk silicon processes. An ordinary digital IC process will produce low Qu in spiral inductors. CMOS or BiCMOS RFIC processes can achieve higher Q inductors by using thicker dielectrics and thicker metal. Q values in the range of 5 to 15 are typical.

The low conversion gain is also due in both cases to an unmatched input. We will consider this later.



RD = 2.5 RL = 400

Unfortunately, for realistic unloaded inductor Q values (on bulk Silicon) of the order of 5, the benefits of tuned output are diminished. The conversion gain is improved by about 4 dB and the noise figure by only 0.5 dB. There would be much more benefit on a CMOS RF Analog, SOI or GaAs processes where higher Q values can be obtained.

Having said that, we will continue to evaluate the tuned solution.



The next step will be to convert the RF output from a differential signal to singleended with an active balun. You must perform this conversion rather than just taking one output from the mixer because the mixer differential output is necessary for rejection of LO feedthrough. Since we need a SAW filter between the mixer output and the driver stage, a single-ended output is sufficient. While passive baluns can be made for 1.8 GHz, we will benefit in cost and size by placing an active balun on-chip. This differential amplifier stage is used to convert the differential output of the tuned mixer to a single output. The gate capacitances of the D2SE stage can be absorbed into the resonator at the mixer drain nodes. The D2SE stage must also be designed so that it does not dominate the IMD generation of the mixer. R_{s_D2SE} can be adjusted to set the V_{1dB} level.

The output driver could use an off-chip load resistor with open drain output connection as suggested by the circuit simulated here. The load resistance will probably be determined either by the filter impedance or by transmission line impedance. The bias current for the D2SE converter stage will be dictated by this impedance level. The device widths must also be chosen so that they can handle the necessary drain current and provide adequate voltage gain. The addition of a source follower to the output is another option.



For the initial design evaluation, we will continue to measure the differential output so that comparisons can be made between the differential tuned mixer and the mixer with output buffer. Then, the mixer will be evaluated in a single-ended configuration.



The SSB noise figure simulation is performed again with parameter sweeps for RS and Rind. We can see that there is little noise sensitivity to Rind, however, it strongly affects the conversion gain. RS affects both NF and conversion gain and it also will also affect the carrier-to-IMD ratio vs. IF input voltage.



The Mixer TOI/IMD simulation is performed again for RS of 10, 20, and 30 ohms. We can see that the dynamic range slowly improves for smaller RS. This will be very dependent on the noise bandwidth, however. For our simulations, a 30 MHz bandwidth was assumed.



A DesignGuide schematic intended for evaluation of single-ended mixers was copied from the menu and modified. Our tuned mixer with the D2SE output stage was inserted from the component library. Unused inputs were terminated: the input was grounded and the output terminated in a large resistance.

The LO is differential. A transformer and source was copied from a differential test schematic and pasted into this schematic. An active LO SE to differential stage could also be designed and added to the mixer if desired.



Again, noise figure and IMD vs RF power sweeps were performed for a range of RS values from 10 to 30 ohms. This is combined to determine dynamic range on the next slide.



The best result was for the RS = 10 ohm case. We see a peak dynamic range of 57.5 dB at an input voltage of 14 mV.



A more severe test of linearity requires simulation with a digital signal source such as this CDMA example. An IS-95 CDMA source with very good ACPR was used to drive the mixer input. When the input RF signal level was set to the optimum value for mixer dynamic range, relatively little spectral regrowth is observed. To save time, only 128 symbols were used in the circuit envelope simulation. A more accurate simulation might require in excess of 1000 symbols.



When the signal level is increased, there is much more distortion evident. The input level in this simulation corresponds to about 30 mV of drive voltage.

| | IF Spect, Isolation | Conv. Gain, PortImpedance | 15 | |
|--|---|--|------------------------|--|
| The RF input port generation is from | impedance can n off-chip. | be matched if bas | seband/IF | |
| We can see at 200 | 0 MHz, the input | impedance is do | minated by | |
| capacitive reactai | 100. | | | |
| | | | | |
| Reference Impedar | nce for Rho | ap 70=50 | | |
| Reference Impedar (refelection coefficie VSWR calculations | nce for Rho ent) and | qn <mark>Z0=50</mark> | Port | |
| Reference Impedar (refelection coefficie VSWR calculations | nce for Rho ent) and E Looking ir | an <mark>Z0=50</mark> nto the RF (Input) | Port: | |
| Reference Impedar (refelection coefficie VSWR calculations Frequency | nce for Rho ent) and E Looking ir Impedance | <mark>qn</mark> Z0=50 nto the RF (Input) Reflection Coefficient | Port: VSWR | |
| Reference Impedar (refelection coefficie VSWR calculations Frequency 200.MHz | nce for Rho ent) and Looking ir Impedance 8.47 - j1.40E2 | nto the RF (Input) Reflection Coefficient 0.96 / -39.20 | Port: VSWR 52.28 | |

We noted earlier that the input of the mixer is badly mismatched. This may not be of much concern if the baseband and IF driver circuits are on the same chip with the upconversion mixer. In that case, the voltage levels are more of interest.

If you are interested in driving from off chip, we can see above that the input impedance is dominated by capacitive reactance. A matching network could increase the conversion gain significantly if this were of interest.



The Mixer DesignGuide contains several impedance matching utilities that could be used to design and evaluate matching networks.



We have now completed a design study of an upconversion transmit mixer. The procedure illustrated here is by no means unique, and you may find ways of getting the same information by other sequences of steps.

Also, the DesignGuide analysis schematics can be further modified to include nested sweeps. These can provide a two-dimensional perspective on the design space to gain further insight (in exchange for increased simulation time and data file size).

You can also make use of the ADS optimizer to automatically achieve the design goals. This could require combining the simulations on more than one analysis schematic onto a single multi-level schematic, or possibly creating a look-up table and interpolation function for one of the critical performance parameters to speed up the optimization process.

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