Colpitts Oscillator Tutorial

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1 ABSTRACT

This paper will describe the design and test of a low noise VHF Colpitts voltage controlled oscillator (VCO), designed to operate at 200MHz (Tuning bandwidth of 2-3MHz/V over 1 to 10V) with an associated phase noise performance of <-100dBc/Hz @ 10KHz.
Theory will be given for the design of the reflection amplifier and high 'Q' resonator, together with the relevant CAD simulations to verify the design.

2 DESIGN DESCRIPTION

2-1 RESONATOR DESIGN [1,2]

The first part of the design process is to determine the required unloaded Q of the resonator to achieve the phase performance of <-100dB/Hz at 10KHz. The simulation shown in **Figure 1** simulates the phase noise of an oscillator for a given loaded Q, Noise figure and frequency. The resulting simulation plot for a VCO at 200MHz with a loaded Q of 30 is shown in **Figure 2**.

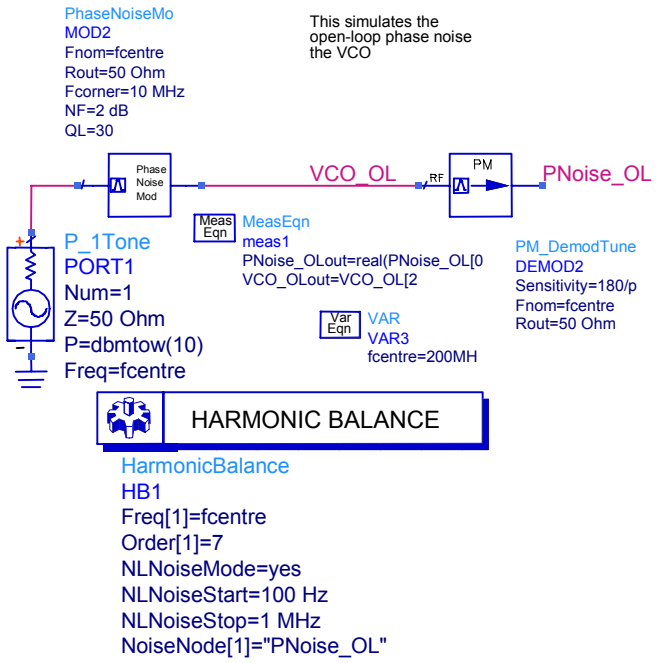


Figure 1 ADS simulation to determine the minimum loaded Q of the resonator required to meet a specific phase noise requirement.

Now that we have a design criteria for the resonator loaded Q (in this case > 30) we could decide on the topography of the resonator.

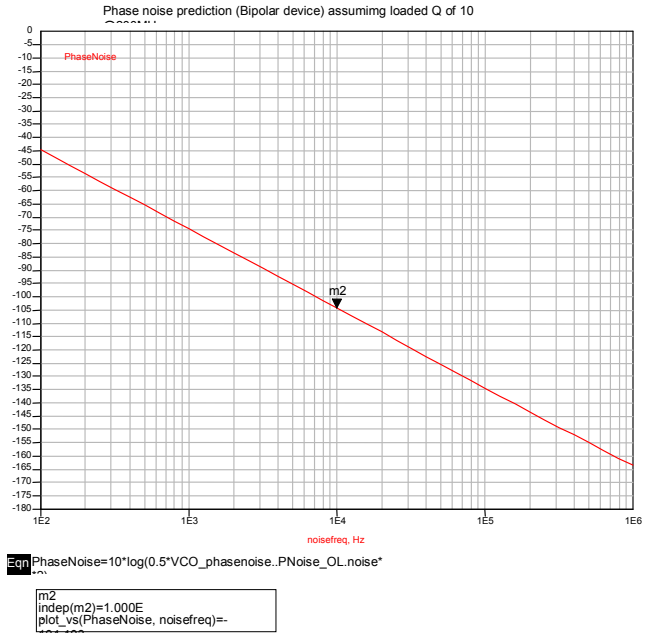


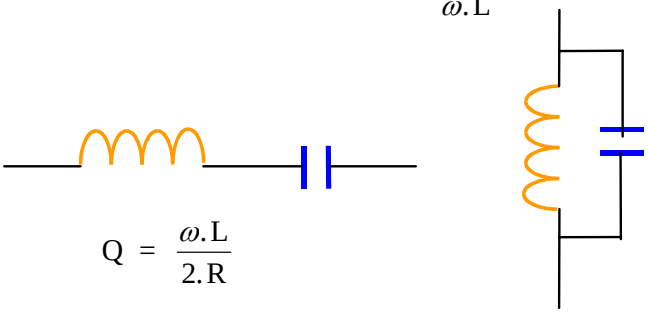
Figure 2 Resulting simulation of the ADS schematic shown in Figure 1, showing a predicted phase noise of –94dBc/Hz at 10KHz for a loaded Q of > 30.

The unloaded/loaded Q of the resonator depends on the values of the L/C ratio of the tank circuit and on the unloaded Q's of the individual components. Typically, ceramic microwave capacitors such as the ATC100a range (by American technical ceramics) have unloaded Q's of between 200 and 1000 with capacitor values up to 10pF. Unfortunately inductor Q's are considerably less, for example the Coilcraft 0805CS series have unloaded Q's of between 50 – 60 and thus are the limiting factor on resonator loaded Q.

2-2TWO ELEMENT RESONATOR CIRCUIT [2]

Figure 3 shows a schematic diagram of a two-element resonator. This circuit is seldom used in oscillators as the loaded Q will be very low as the source and load impedances will directly load the tuned circuit.

$$Q = \frac{2.R}{\omega.L}$$



$$Q = \frac{\omega.L}{2.R}$$

Figure 3 Schematic of a two element, lumped resonator, together with loaded Q equations. The 2R assumes that the circuit is terminated in both a source and load impedance (value R)

At resonance the transmission phase is zero and the network is loss less (except for the resistance of the inductor). The series resonator impedes signal transmission while the parallel network allows signal transmission. The main problem with such a simple resonator is achieving a required Q, for example if we want a Q of 30 we would need the following series inductor & capacitor at 200MHz:

$$L = \frac{2.R.Q}{\omega} = \frac{2 * 50 * 30}{2\pi * 200E^{6}} = 2.3uH$$

$$C = \frac{\left(\frac{1}{2\pi f}\right)^{2}}{L} = \frac{\left(\frac{1}{2\pi * 200E^{6}}\right)^{2}}{2.3E^{-6}} = 0.27pF$$

The problem with this circuit is that the loaded/unloaded Q and phase of the network are interdependent and therefore it is better to lightly couple the resonator by using a capacitor so that the unloaded Q of the resonator is effectively separated from the load impedance load, which would normally greatly reduce the Q of the resonator.

The addition of the coupling capacitor Cc to the resonator, will allow us to change the loaded Q of the circuit without greatly effecting the resonant frequency. This arrangement is shown in **Figure 7**. In addition if frequency control is required then the varactor network shown can be added in parallel with the tuned circuit.

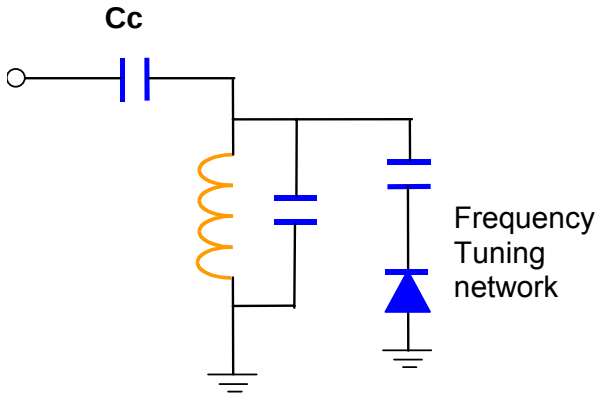


Figure 4 Modified L-C resonator with Coupling capacitor Cc added to isolated the unloaded Q of the resonator with the applied load. In addition the varactor network can be added to give frequency tuning. The bandwidth of the frequency controlled network is adjusted by the capacitor in series with the varactor.

The easiest way to determine the maximum Coupling capacitor Cc is by way of the simulation shown in **Figure 5**. **Note** that an arbitrary inductor value has been chosen and the Capacitor C2 is used to resonate it at 200MHz. It is better to have a higher value of resonating capacitor so that the effect of the Coupling Capacitance (Cc) on the resonator frequency is minimized.

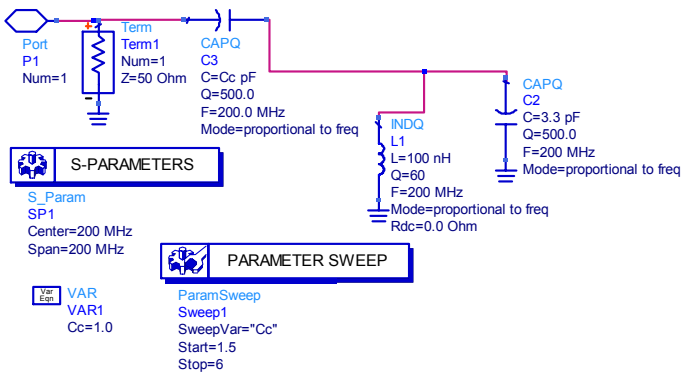


Figure 5 ADS simulation to vary the value of Cc to determine the resonator loaded Q. Note the S-parameter block needs the 'Group Delay' parameter checked.

The resulting simulation plot is shown in **Figure 6**. The plots show us that if we require a loaded Q of > 30 then Cc must be less than 2.5pF. But we have to remember that Cc will also effect the phase looking into the resonator which we have to equal to the reflection amplifier phase but with opposite sign. In addition the varactor network will effect the loaded Q and resonator frequency depending on the coupling to the varactor. This coupling determines the capacitance swing and hence tuning bandwidth of the resonator. So a narrow tuning network gives the better Q than a wideband network.

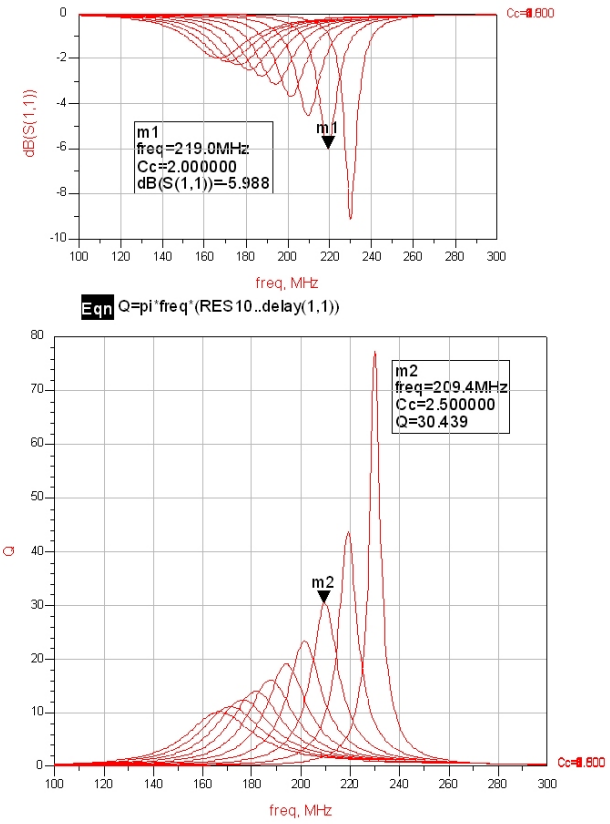


Figure 6 Result of simulation shown in Figure 5, showing variation in loaded Q with Coupling capacitor Cc (varied between 1.5pF & 6pF in 0.5pF steps). If we require a loaded Q of > 30 then Cc must be less than 2.5pF.

Now that we have determined our basic resonator design we need to determine the values of the varactor network, by choosing a varactor and the correct coupling capacitor to give us the correct delta C for the resonator. From the varactor data sheet we can note the capacitance vs voltage curve and thus generate a varactor model for use in our simulations.

2-3VARACTOR MODEL AND TUNING RANGE [3]

Voltage variable capacitors or tuning diodes are best described as diode capacitors employing the junction capacitance of a reverse biased PN junction. The capacitance of these devices varies inversely with the applied reverse bias voltage and is used to vary the centre frequency of the resonator. The equivalent circuit of a typical varactor together with the package parasitics is shown in **Figure 7**.

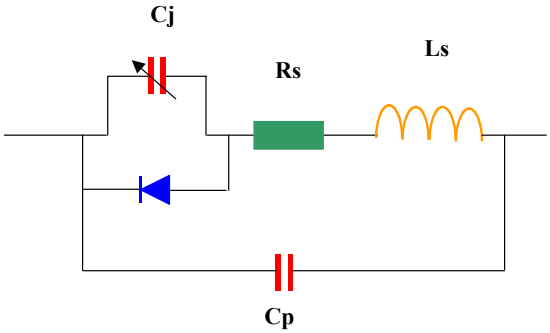


Figure 7: Typical equivalent circuit of a varactor diode. The series inductor Ls and parallel capacitor Cp are package parasitics, typical values are Cp ~ 0.1pF and Ls = 1.5nH.

The general equation for calculating the capacitance of the varactor is:

$$C_V = \frac{C_J}{\left(1 + \frac{V_R}{V_J}\right)^{\gamma}} + C_P$$

where :

C_V = diode capacitance

V_R = applied voltage,

V_J = junction contact potential (~ 0.7V)

γ = Capacitance exponent

C_V = diode capacitance

For the Philips BB405 varactor diode, Rs is given as 0.75ohms with capacitances of 18pF@1V, 11pF@3V and 2pF@28V. For the above equation the capacitance values equate to a value of $\gamma = 0.74$ with CJ = 35pF (valid for control voltages 1 to 28V) . The varactor model was substituted for the fixed capacitor and simulated over a range of tuning voltages to determine the frequency range and tuning constant of the resonator. The easiest way to determine the value of the coupling capacitor is to generate a spreadsheet and enter values of Varactor coupling capacitor as shown in **Table 1**. From the table we can see that if we pick a varactor coupling capacitor of 6pF then we should achieve our tuning bandwidth of ~ 3MHz/V. Note the addition of the resonator coupling capacitor Cc will alter these values slightly and some adjustments may need to be made.

Varactor Max Cap	**14 pF**	1.4E-11
Varactor Min Cap	**4 pF**	4E-12
Enter Tuning range	**10 V**	
Resonator Cap	**2.7 pF**	2.7E-12
Resonator Ind	**100 nH**	0.0000001

Varactor coupling Cap (pF)	Varactor Network Max C	Min C	Min Freq (MHz)	Max Freq (MHz)	Tuning Range (MHz/V)
0.5	0.482759	0.444444	282	284	0.17
1	0.933333	0.8	264	269	0.50
2	1.75	1.333333	239	251	1.20
3	2.470588	1.714286	221	240	1.82
4	3.111111	2	209	232	2.34
5	3.684211	2.222222	199	227	2.77
6	**4.2**	**2.4**	**192**	**223**	**3.13**
7	4.666667	2.545455	185	220	3.43
8	5.090909	2.666667	180	217	3.69
9	5.478261	2.769231	176	215	3.92
10	5.833333	2.857143	172	213	4.12
11	6.16	2.933333	169	212	4.30
12	6.461538	3	166	211	4.45
13	6.740741	3.058824	164	210	4.59
14	7	3.111111	162	209	4.72
15	7.241379	3.157895	160	208	4.83

Table 1 Result of spreadsheet calculation of varactor coupling capacitor on frequency and tuning bandwidth. If we pick a varactor coupling capacitor of 6pF then we should achieve our tuning bandwidth of ~ 3MHz/V. Note the addition of the resonator coupling capacitor Cc will alter these values slightly and some adjustments may need to be made.

We can now put all the components together and simulate the frequency response, Q and tuning range of the resonator before designing the reflection amplifier. For the next simulation shown in the varactor sub-model has been added, which is shown in **Figure 8** and a symbol was generated for use in the resonator model shown in **Figure 9**.

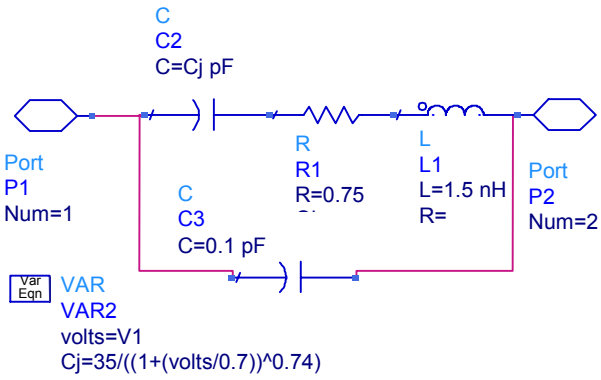


Figure 8: ADS sub-model of the BB405 varactor diode. The voltage V1 is passed through to this model at a higher level.

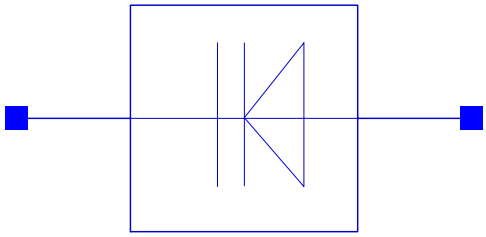


Figure 9 Using the view – create/edit schematic symbol command in ADS, this diode symbol was drawn for use in the resonator network model.

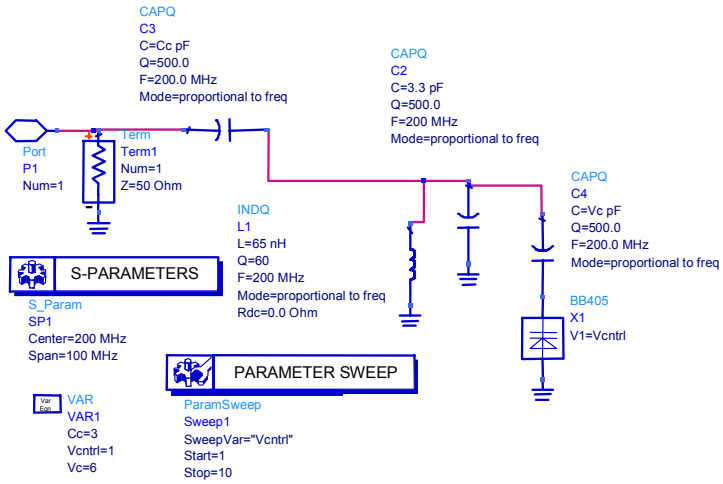


Figure 10 ADS schematic of the completed resonator. The sweep parameter box is set to sweep the varactor control voltage between 1 – 10V and is fed through to the varactor model by V1=Vcntrl. (Note to set the through variable right click on the varactor symbol and select 'edit component parameters' then add the variable V1=Vcntrl). In order to get the correct resonant frequency with the varactor network and coupling capacitor Cc added – the inductor was reduced in value from 100nH to 65nH.

The simulated sweep of Q/frequency vs control voltage (Vcntrl) is shown in **Figure 11**. We can see from the top plot of input return loss (S11) that we need to design a reflection amplifier with at least 8dB of reflection gain to overcome the losses of the resonator. Usually the reflection amplifier is design with greater gain > 3dB extra to give some margin.

The next section will now deal with the design of the reflection amplifier part of the colpitts oscillator design.

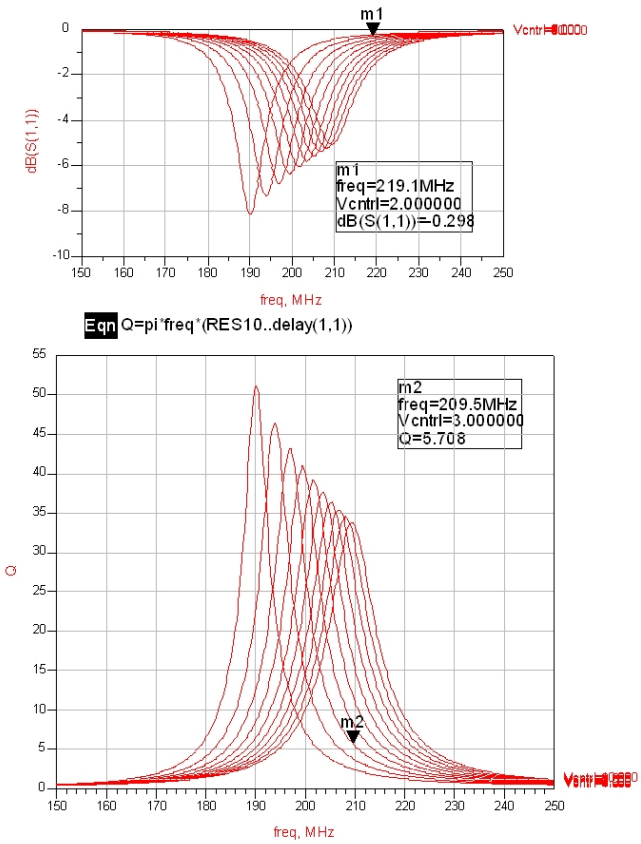


Figure 11 The completed resonator plot of Q vs sweep control voltage (Vcntrl). We can see from the top plot that we need to design a reflection amplifier with at least 8dB of reflection gain to overcome the losses of the resonator.

4.8 REFLECTION AMPLIFIER DESIGN [4,5,6]

The reflection amplifier of the Colpitts oscillator was achieved by the use of capacitive feedback network as shown in **Figure 12**.

A suitable RF medium power bipolar transistor, with a ft of > 1GHz was required and at this low frequency there were several to choose from including the BFR92, BRF93, BFY90 and AT41435.

For this design the BFR92 was chosen.

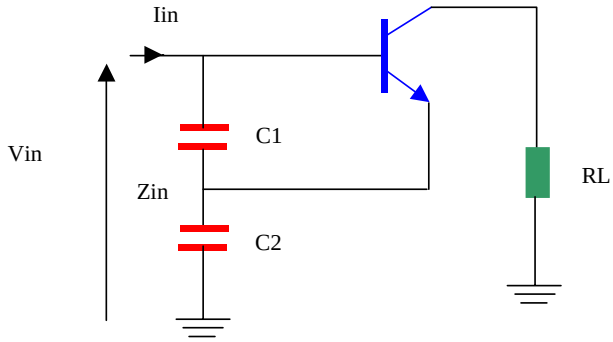


Figure 12: Simplified schematic diagram showing the reflection amplifier part of the Colpitts oscillator. The capacitor network of C1 and C2 would provide positive feedback from the emitter to base.

The steady state loop equations were expanded out, (as shown in the **Colpitts derivation tutorial**) to yield an expression for the negative impedance of this type of amplifier, in terms of the capacitors used for feedback and the transconductance of the active device:

$$\frac{Vin}{Iin} = Zin = -gm.\frac{1}{\omega C_1 C_2} + \frac{1}{j\omega[C_1 C_2 (C_1 + C_2)}$$

Input impedance (negative) Parallel combination of C1 & C2

And

$$fo = \frac{1}{2\pi\sqrt{L[C_1.C_2(C_1 + C_2)]}}$$

As we assumed that XC_1 << *hie*, then C1 should be as large as possible and in order for these feedback components to dominate over the parasitic capacitance's of the transistor C2 should be as large as possible too.

$$\text{For sustained oscillation } Rs = \frac{gm}{\omega^2.Cm^2}$$

Assuming $C1 = C2$ then Cm is the product of the two capacitance's.

Although we required large values of capacitance to dominate the circuit performance, they were restricted in their size by the following expression:

$$Rs \le \frac{gm}{\omega^2.Cm^2} \le \frac{G}{\omega^2.Cm^2} \quad \text{re - arranging : -}$$

$$Rs \le \frac{G}{\omega^2.Cm^2} \qquad \frac{Rs}{G} \le \frac{1}{\omega^2.Cm^2} \qquad \sqrt{\frac{Rs}{G}} \le \frac{1}{\omega.Cm}$$

Where G is the maximum value of gm -
(the transistors mutual conductance)
& Rs is the input impedance of the resonator

By simulation of the Spice model – BFR92 at various collector currents, the input resistance (*hie*) and AC current gain (hfe) were determined, in order to calculate the values of gm and G as given in the previous equations. **Figure 13** below shows the HP ADS circuit used to analyse the required parameters and **Table 2** shows the resulting values of *hie* and *hfe*, for a current of 5mA (Rload = 1150 ohms):

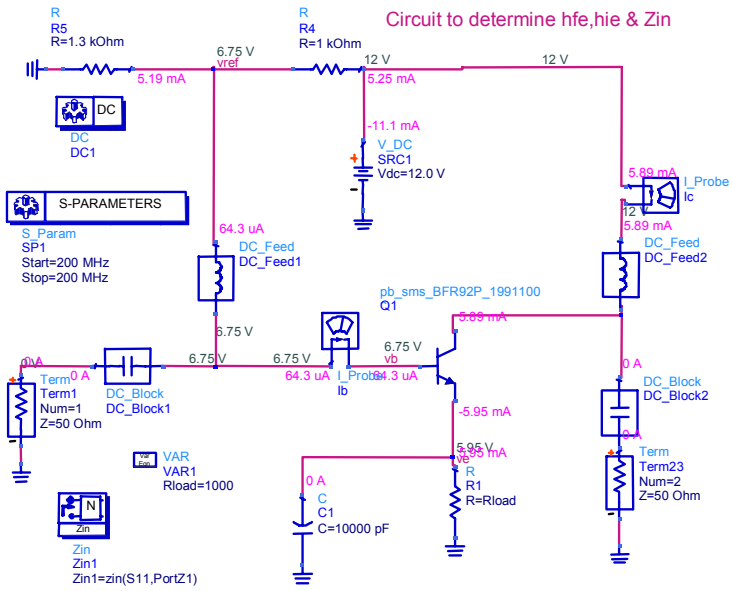


Figure 13: HP ADS circuit used to analyse the necessary parameters required calculating the feedback capacitors C1 & C2. To calculate *hfe* & *hie* the values of Ic, Ib, vin & ve were analysed - *hfe* = Ic/Ib and *hie* = (vin-ve)/Ib. By RF decoupling the emitter of the transistor, (by use of C1) the input impedance at 200MHz was predicted, by running an S-parameter simulation on the circuit.

			mA/V	Rin (ohms)
Ic.i	hfe	hie	gm	Zin1
5.000mA	91.293	14378.439	6.349	78.695 / -56.883

Eqn hfe=Ic.i/Ib.i Eqn hie=(vb-ve)/Ib.i Eqn gm=(hfe/hie)*1E3

Table 2 Simulation output & equations for the ADS simulation shown in Figure 13

By running the simulation with different values of Rload a range of parameters are calculated so that the colpitts capacitors can be calculated for a particular current. The table of various Rload settings is shown in **Table 3**.

Ic (mA)	Rload (ohms)	Rin (ohms)	hfe	Zin (ohms)	Gm (mA/V)
2	2970	34014	89	41	2.6
5	1180	14378	91	43.9	6.4
7	840	10473	91.7	43.7	8.76
10	580	7422	92.2	42.2	12.5
12	485	6290	92.5	42.5	14.7
15	385	5085	92.7	42.7	18.3
18	320	4293	92.86	42.4	21.6
20	285	3863	92.9	42.4	24
22	260	3555	93	41.8	26
25	229	3170	93.1	42.5	29

Table 3 Simulation summary of the basic amplifier circuit of Figure 13 for various values of Rload. Values of Input resistance (hie) and (AC Gain) hfe for the BFR92 transistor for various collector current bias values. Using this data the value of gm was calculated.

Using the values shown in **Table 3**, we could estimate the maximum series capacitance of the combination of C1 and C2 i.e. Cm at a picked current of 5mA

Note the input impedance of the resonator Rs can be found be re-simulating the resonator with a Zin block and for our example Rs = 17 ohms

$$\frac{1}{\omega.Cm} \ge \sqrt{\frac{r}{gm}} \quad \text{at Ic} = 5\text{mA} \qquad \sqrt{\frac{17}{6.4E^{-3}}} = 51$$

$$\text{At 200MHz} \quad Cm \le \frac{1}{2\pi.200E^{6}.51} \le 15\text{pF}.$$

Using initial values of C1 and C2 = 30pF, the reflection amplifier was analyzed using HDADS and the circuit shown in **Figure 14**. The two feedback capacitors were optimised to produce a reflection gain > 12dB and resulted in capacitor values of 33pF for C1 and C2. This circuit included the spice model of the BFR92, which required biasing to a voltage supply via the RF bias components for the simulation to work. A S-parameter analyser box, was added to the schematic to allow the reflection magnitude and phase to be plotted while, the addition of the DC analyser box allowed DC bias conditions to be predicted at each node.

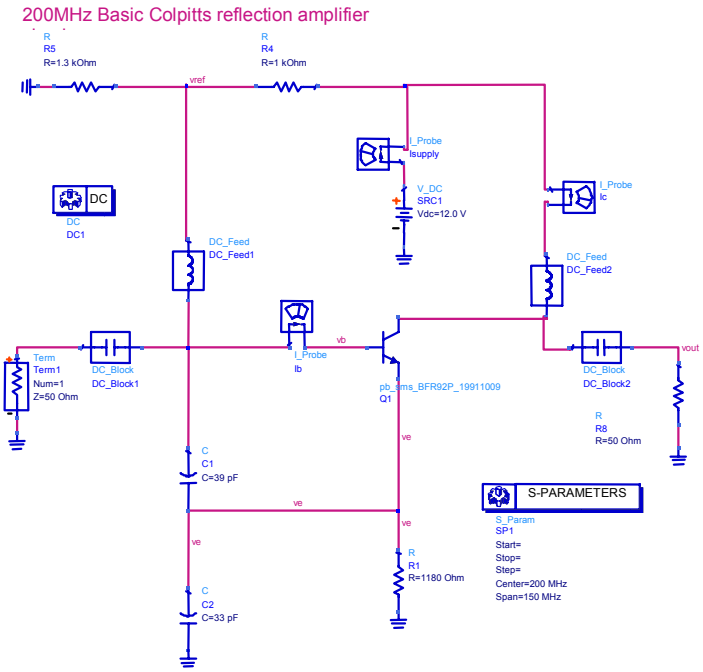


Figure 14: Circuit used to analyse the reflection amplifier, with the additions of the 'ideal' bias components. An S-parameter simulation is run to determine the frequency response of the reflection amplifier's return gain, together with the corresponding value of reflection phase.

Figure 18 Shows the frequency response of the reflection amplifier part of the Colpitts with the feedback capacitors both set to ~ 33pF. The aim was to maximise the 'reflection gain' at the centre frequency of 200MHz, by varying the values of C1 and C2. This return gain must end up being greater than the return loss of the resonator and in addition, the phase of the resonator must be opposite to the input phase of the reflection amplifier, to ensure oscillation will occur.
The circuit was optimised to maximise the gain of the reflection amplifier. This occurred with values of capacitors C1 = 33pF and C2 = 33pF, resulting in a reflection gain of 13.8dB, with a corresponding reflection phase of –67 degrees.

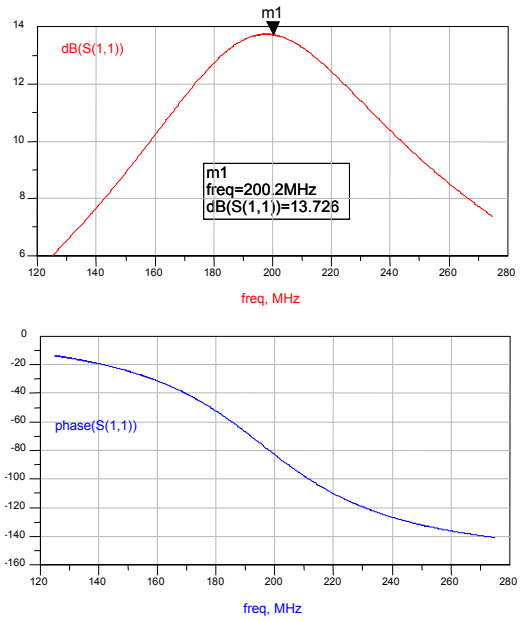


Figure 15 CAD analysis of the reflection amplifier with the input bias inductor tuned for best reflection gain. The plot on the left shows return 'gain' in dB and the plot on the right shows the return phase in degrees both at 200MHz. With these values of gain there was a ~ 6dB gain margin when the resonator was coupled to the amplifier.

The final phase and input return loss plots of the resonator set to the middle of the band ie 200MHz (with a control voltage of 4.3V) is shown in **Figure 16**.

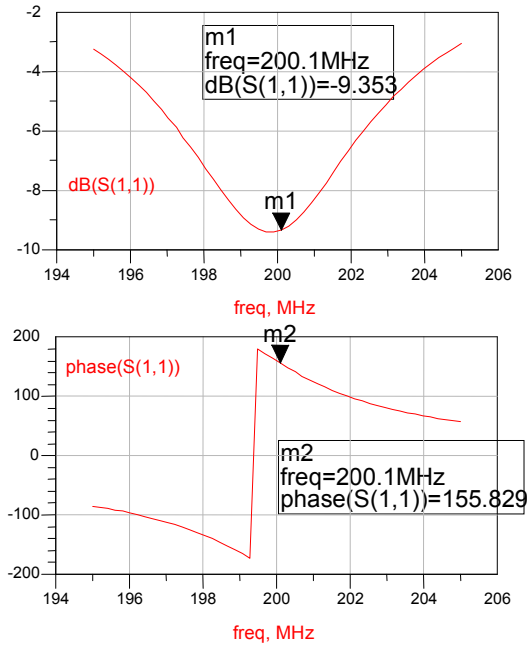


Figure 16 Shows the phase of the resonator with the control voltage of the varactor set to give a frequency of 200MHz. The resulting phase is +155 degrees with a return loss of 9.4dB

4.9 OSCILLATOR SIMULATION

When the two circuit elements (resonator & reflection amplifier) are connected together that the loop phase will be zero. Analysis of the resonator and the reflection amplifier, yielded reflection phases of +155 and –67 degrees respectively. However, the reflection phase of the resonator already *includes*, the coupling capacitor required to give the correct loaded 'Q'. For oscillation to occur, there must be >1 magnitude at the zero phase point. Ideally this should occur at maximum reflection gain for best performance.

The easiest way to evaluate this capacitance & frequency of oscillation is to perform a S-parameter measurement with the resonator and reflection amplifier connect together as shown in **Figure 17**.

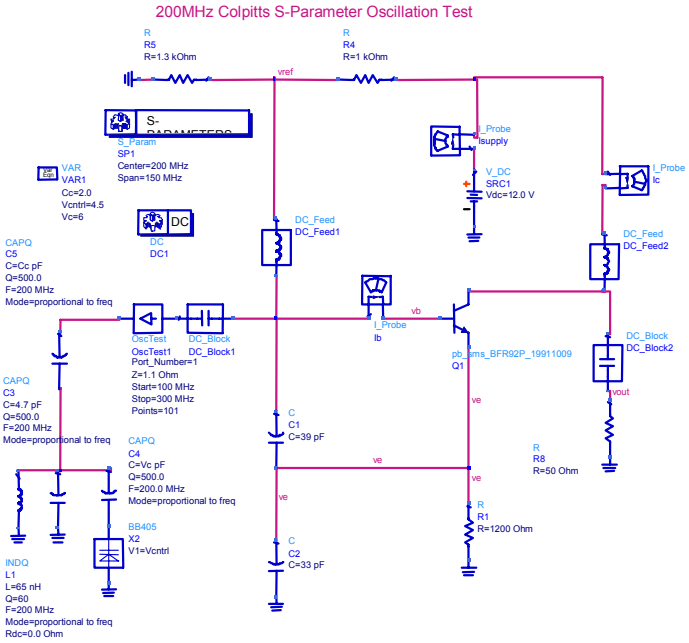


Figure 17 S-Parameter simulation of the completed Colpitts oscillator. The Osctest block has been placed between the resonator & reflection amplifier in order to determine the magnitude & gain at a particular frequency. That's is to say we require a magnitude greater than 1 at zero phase at the operating frequency for oscillation to occur.

With the OscTest simulator block connected between the resonator and reflection amplifier we can simulate the combined phase and magnitude at the oscillation frequency. The result of the simulation is shown in **Figure 18**.

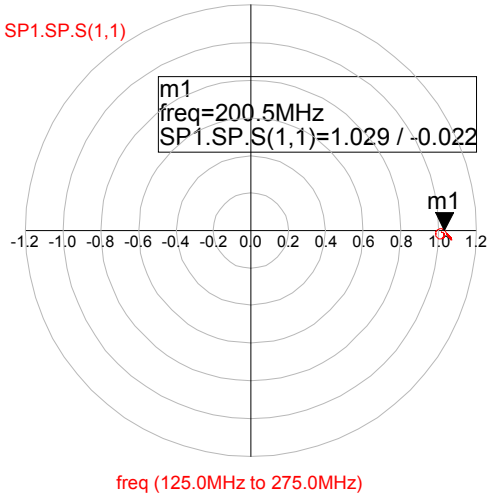


Figure 18 Result of the simulation shown in Figure 17. Showing that at 200MHz we do indeed have a phase of zero and a magnitude greater than 1. (Note the resonator capacitor C3 was adjusted to give the correct oscillation frequency with the varactor set for mid tuning range.

With the circuit verified for oscillation at 200MHz, we could now simulate the two circuits together using non-linear analysis to obtain phase noise, output power, harmonics and DC bias values. The simulation shown in **Figure 19** uses a Harmonic Balance simulator to simulate phase noise, output power and frequency performance. A number of parameters need to be set in the harmonic balance simulator box ie:

Freq: 200MHz , order 3.

Noise(1): Select Log, Start 100Hz, Stop 10MHz, Points/decade 10, Select Include FM noise.

Noise(2) Select "vout", Select Non linear Noise & Oscillator

Osc Osc Port name "Osc1"

All other parameters can be left to their default values.

The simulation model contained the reflection amplifier based around a 'spice' model of the BFR92 together with associated DC bias.

Note: To make the simulation more accurate and representative of a final design, transmission lines should be added for the component pads and circuit inter-connections.

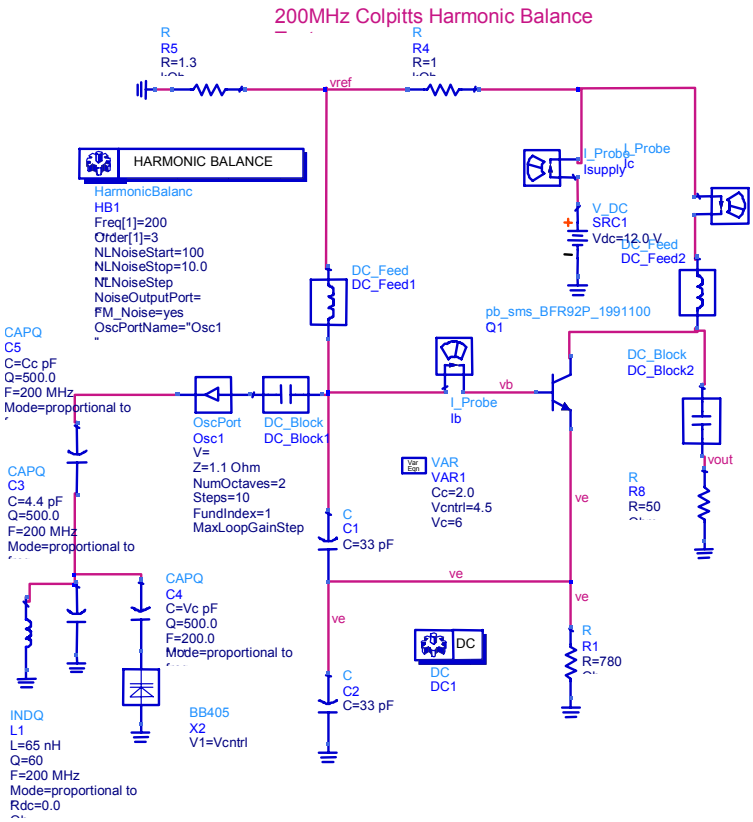


Figure 19: Harmonic balance ADS schematic of the Colpitts oscillator. The Colpitts feedback capacitors and resonator tuning capacitor have been optimized for frequency and oscillator output power. The simulator uses the 'Oscport', to inject RF into the system to allow prediction of oscillated frequency, power and phase noise.

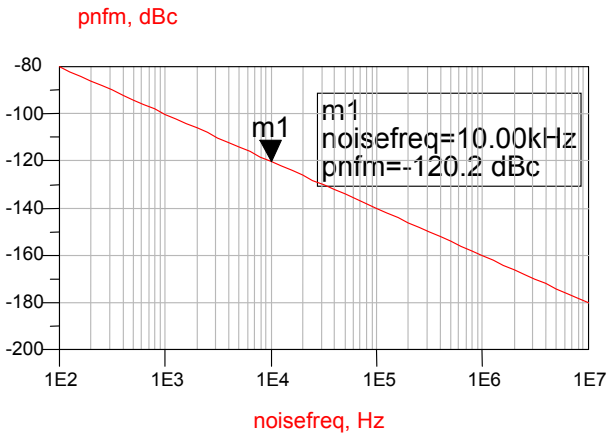
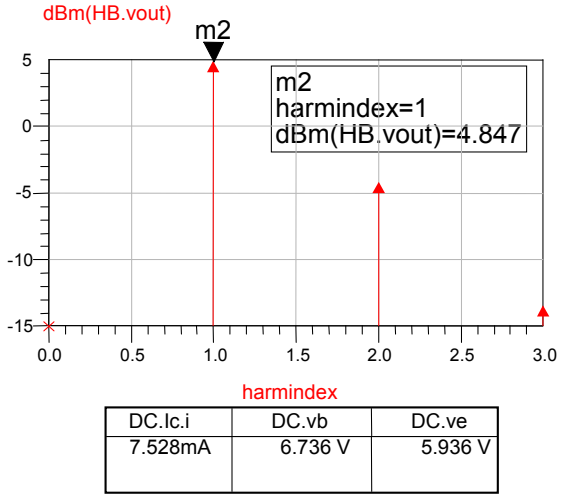


Figure 20: Predicted phase noise plot showing phase noise in dBc/Hz against carrier offset frequency in Hz. The red line is the simulation result with the blue line showing the required specification. The oscillator was designed to meet the phase noise specification with a 20 dB margin. In practice the close to carrier phase noise i.e. < 1KHz will be at least 10dB worse than the simulation due to the device flicker noise which is not defined in the BFR92 spice model. Any phase noise below about –150dBC/Hz was unlikely to be measured as this level fell below the measuring system noise floor.



DC.Ic.i	DC.vb	DC.ve
7.528mA	6.736 V	5.936 V

Figure 21: Harmonic level output simulation showing harmonic output power (dBm) against the harmonic index. The marker is set to the oscillator fundamental frequency (index=1). The relatively high second harmonic level required that the following buffer amplifier was fitted with some form of harmonic filter either as part of the output matching circuit or a stand alone low-pass filter.

harmindex	HB.freq
0	0.0000 Hz
1	200.2MHz
2	400.4MHz
3	600.6MHz

Table 4: Harmonic index against output frequency. This table shows the frequencies of the various harmonic indices given in the simulation at the top of the page.

8 SUMMARY AND CONCLUSION

The VCO met the requirements of the equipment specification except for the VCO tuning bandwidth, which was slightly low at by ~ 2.2MHz - Ideally to give a bit of margin needs to be ~ 2.5MHz/V. This could be increased by increasing the varactor coupling capacitor to the next preferred value.

To complete the design a VCO buffer amplifier complete with harmonic filter needs to be designed to reduce the output power variations over temperature and remove any load-pulling effects (i.e. a change in oscillating frequency with variations in the output load/match). To eliminate load-pull between the VCO and buffer amplifier, an attenuator can be fitted before the buffer amplifier (still ensuring that the buffer amplifier is operated in compression). With the buffer amplifier in compression, (or in limiting) the variations in the VCO output power with temperature and control voltage should be greatly reduced.

10 REFERENCES

[1] Radio Frequency Design – Wes Hayward, 1994, The American Radio Relay League, ISBN 0-87259-492-0, p262.

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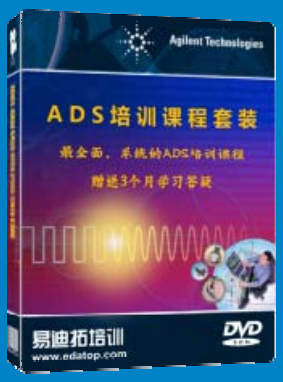

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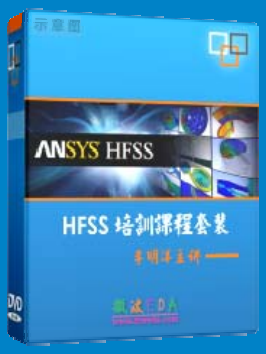

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