Freescale Semiconductor's MET LDMOS Model

1. Description of the Model

The MET LDMOS model [1] is an electro thermal model that can account for dynamic self-heating effects and was specifically tailored to model RF high power LDMOS transistors and RF ICs used in base station, digital broadcast, land mobile and subscriber applications. It has been implemented in Agilent EEsof ADS™ harmonic balance simulator and is capable of performing small-signal, large-signal, harmonic-balance, noise and transient simulations.

The MET model is an empirical large signal nonlinear model, which is single-piece and continuously differentiable and includes static and dynamic thermal dependencies. This new model is capable of accurately representing the current-voltage characteristics and their derivatives at any bias point and operating temperature. A single continuously differentiable drain current equation models the subthreshold, triode, high current saturation and drain to source breakdown regions of operation. A set of static thermal equations governing the electro-thermal behavior of the drain to source nonlinear current model parameters were developed by measuring the nonlinear drain current under pulsed voltage conditions at different operating temperatures, ensuring an isothermal measurement environment.

Pulsed S-parameters were used to develop equations to model the capacitance functions of voltage and temperature, which were described by functions that have no poles and facilitate robust numerical stability. The nonlinear capacitances were extracted with a small signal model that represents the small signal limit of the device nonlinear behavior at any given bias point. Using a thermal analogue circuit, as in many previous circuit models, the MET LDMOS model accommodates thermal effects. The self-consistent temperature determined by this circuit sets the values of current control parameters, capacitance values and source, drain and gate resistances.

2. Equivalent Circuit

The large signal equivalent circuit of the MET LDMOS model is shown in Figure 1. The model has one voltage and temperature dependent nonlinear current source, Ids, as well as a forward diode and a reverse diode. The forward diode is a function of voltage while the reverse diode is temperature and voltage dependent. The reverse diode has a temperature dependent series resistance associated with it. The model also has three voltage and temperature dependent nonlinear charges, Qgs, Qgd, and Qds. There are two internal gate conductances, Ggs, and Gdg as well as three temperature dependent parasitic resistances, Rg, Rd, and Rs. The instantaneous temperature rise is calculated with the use of the thermal sub-circuit, where Itherm is the total instantaneous power dissipated in the transistor, Rth is the thermal resistance, Cth is the thermal capacitance, and V_tsnk is a voltage source that represents the heat sink temperature of the system. The isothermal small signal equivalent circuit model produced by linearizing the MET LDMOS model is shown in Figure 2.

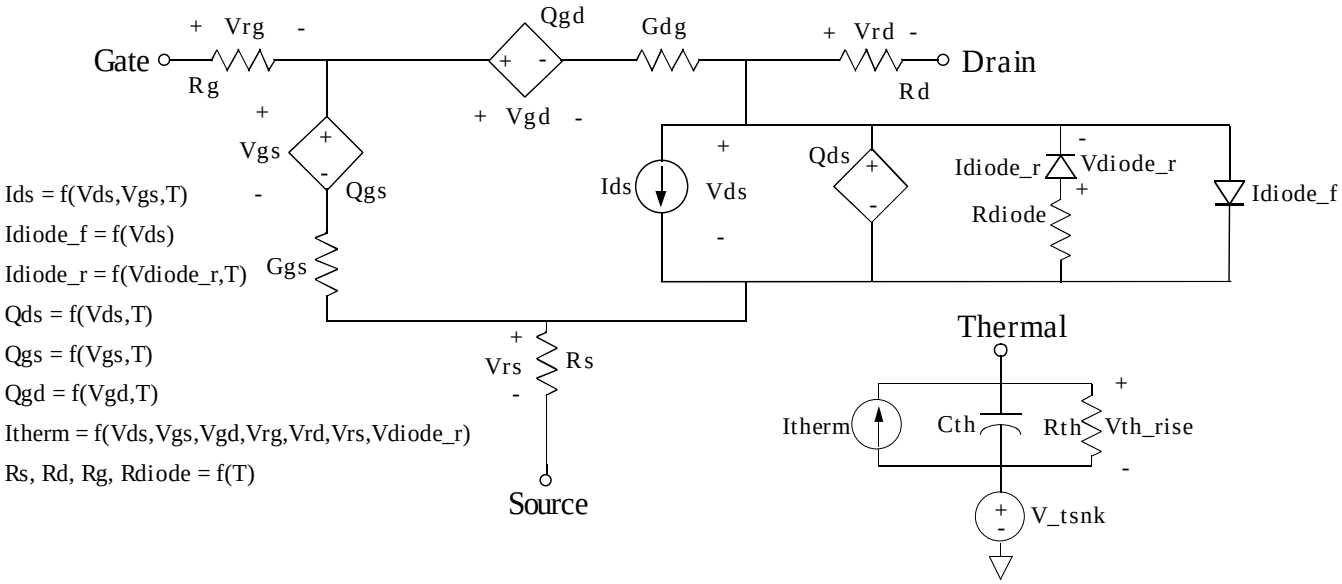

Figure 1. Large Signal Equivalent Circuit of the MET LDMOS model.

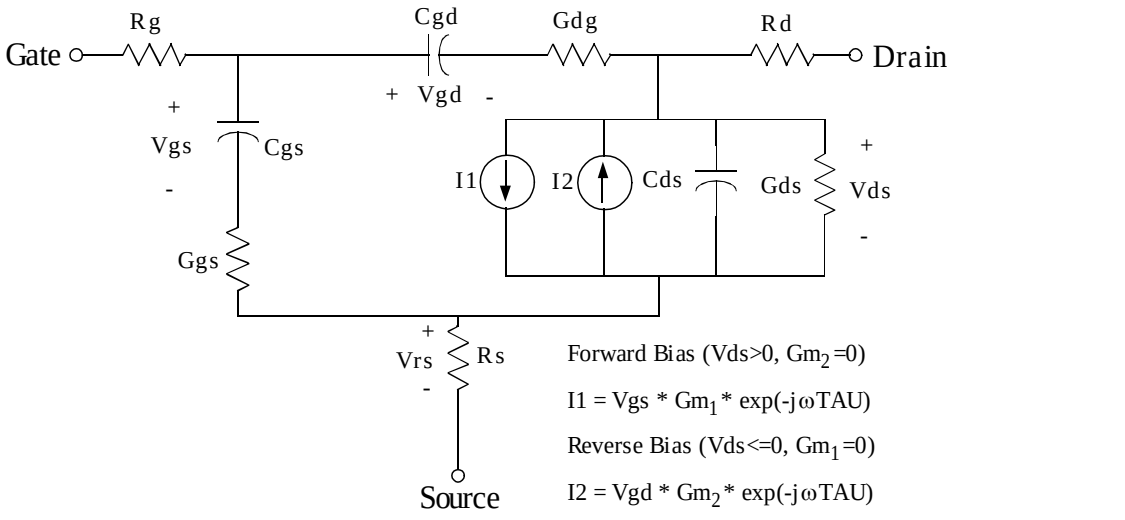

Figure 2. Isothermal Small Signal Equivalent Circuit of the MET LDMOS model.

3. Model Parameters

The following table contains all the MET LDMOS model parameter definitions and their units.

PARAMETER NAME	PARAMETER DEFINITION	DEFAULT VALUE	UNITS
RG_0	Gate Resistance Evaluated at Tnom	1	Ω
RG_1	Gate Resistance Coefficient	0.001	Ω/K
RS_0	Source Resistance Evaluated at Tnom	.1	Ω
RS_1	Source Resistance Coefficient	0.0001	Ω/K
RD_0	Drain Resistance Evaluated at Tnom	1.5	Ω
RD_1	Drain Resistance Coefficient	0.0015	Ω/K
VTO_0	Forward Threshold Voltage Evaluated at Tnom	3.5	V
VTO_1	Forward Threshold Voltage Coefficient	-0.001	V/K
GAMMA	IDS Equation Coefficient	-0.02	---
VST	Sub-Threshold Slope Coefficient	0.15	V
BETA_0	IDS Equation Coefficient. BETA Evaluated at Tnom	0.2	1/Ω
BETA_1	IDS Equation Coefficient	-0.0002	1/(ΩK)
LAMBDA	IDS Equation Coefficient	-0.0025	1/V
VGEXP	IDS Equation Coefficient	1.1	---
ALPHA	IDS Equation Coefficient	1.5	---
VK	IDS Equation Coefficient	7.0	V
DELTA	IDS Equation Coefficient	0.9	V
VBR_0	Breakdown Voltage Evaluated at Tnom	75.0	V
VBR_1	Breakdown Coefficient @ Vgs=0V	0.01	V/K
K1	Breakdown Parameter	1.5	---
K2	Breakdown Parameter	1.15	1/V
M1	Breakdown Parameter	9.5	---
M2	Breakdown Parameter	1.2	1/V
M3	Breakdown Parameter	0.001	---
BR	Reverse IDS Equation Coefficient	0.5	1/(VΩ)
RDIODE_0	Reverse Diode Series Resistance Evaluated at Tnom	.5	Ω
RDIODE_1	Reverse Diode Series Resistance Coefficient	0.001	Ω/K
ISR	Reverse Diode Leakage Current	1e-13	A
NR	Reverse Diode Ideality Factor	1.0	---
VTO_R	Reverse Threshold Voltage Coefficient	3.0	V
RTH	Thermal Resistance Coefficient	10	°C/Watts
GGS	Gate To Source Conductance	1e5	1/Ω
GGD	Gate to Drain Conductance	1e5	1/Ω
TAU	Transit Time Under Gate	1e-12	Seconds
TNOM	Temperature at Which Model Parameters are Extracted	298	K
TSNK	Heat Sink Temp.	25.0	°C
CGST	Cgs Temperature Coefficient	0.001	1/K
CDST	Cds Temperature Coefficient	0.001	1/K

CGDT	Cgd Temperature Coefficient	0.0	1/K
CTH	Thermal Capacitance	0.0	J/°C
KF	Flicker Noise Coefficient	0.0	---
AF	Flicker Noise Exponent	1.0	---
FFE	Flicker Noise Frequency Exponent	1.0	---
N	Forward Diode Ideality Factor	1.0	---
ISS	Forward Diode Leakage Current	1e-13	A
CGS1	Cgs Equation Coefficient	2e-12	F
CGS2	Cgs Equation Coefficient	1e-12	F
CGS3	Cgs Equation Coefficient	-4.0	V
CGS4	Cgs Equation Coefficient	1e-12	F
CGS5	Cgs Equation Coefficient	0.25	1/V
CGS6	Cgs Equation Coefficient	3.5	1/V
CGD1	Cgd Equation Coefficient	4e-13	F
CGD2	Cgd Equation Coefficient	1e-13	F
CGD3	Cgd Equation Coefficient	0.1	$1/V^2$
CGD4	Cgd Equation Coefficient	4	V
CDS1	Cds Equation Coefficient	1e-12	F
CDS2	Cds Equation Coefficient	1.5e-12	F
CDS3	Cds Equation Coefficient	0.1	$1/V^2$
AREA	Gate Periphery Scaling Parameter	1	---
N_FING	Gate Finger Scaling Parameter	1	---

4. Scaling Rules

The model parameters are scaled by two different parameters, AREA, which is the ratio of the desired gate periphery to the gate periphery of the transistor used in the extraction of the model parameters, and N_FING, which is the ratio of the desired number of fingers to the number of fingers of the transistor used in the extraction of the model parameters. [2]

$$AREA = \frac{Znew}{Zextracted} \tag{1}$$

$$N\_FING = \frac{NGates\_extracted}{NGates\_new} \tag{2}$$

where *Znew* and *Ngates_new* are the gate periphery and number of gate fingers respectively of the desired transistor, and *Zextracted* and *NGates_extracted* are the gate periphery and number of gate fingers of the extracted transistor.

$$RD\_0 = \frac{RD\_0}{AREA} \tag{3}$$

$$RS\_0 = \frac{RS\_0}{AREA} \tag{4}$$

$$RG\_0 = RG\_0 * AREA * N\_FING^2 \tag{5}$$

$$RD\_1 = \frac{RD\_1}{AREA} \tag{6}$$

$$RS\_1 = \frac{RS\_1}{AREA} \tag{7}$$

$$RG\_1 = RG\_1 * AREA * N\_FING^{2} \tag{8}$$

$$RDSO = \frac{RDSO}{AREA} \tag{9}$$

$$GGD = GGD * AREA \tag{10}$$

$$GGS = GGS * AREA \tag{11}$$

$$RTH\_0 = \frac{RTH\_0}{AREA} \tag{12}$$

$$C\_TH = C\_TH * AREA \tag{13}$$

$$BETA\_0 = BETA\_0 * AREA \tag{14}$$

$$BETA\_1 = BETA\_1 * AREA \tag{15}$$

$$CGS1 = CGS1 * AREA \tag{16}$$

$$CGS2 = CGS2 * AREA \tag{17}$$

$$CGS4 = CGS4 * AREA \tag{18}$$

$$CGD1 = CGD1 * AREA \tag{19}$$

$$CGD2 = CGD2 * AREA \tag{20}$$

$$CDS1 = CDS1 * AREA \tag{21}$$

$$CDS2 = CDS2 * AREA \tag{22}$$

$$ISS = ISS * AREA \tag{23}$$

$$ISR = ISR * AREA \tag{24}$$

$$BR = BR * AREA \tag{25}$$

$$RDIODE\_0 = \frac{RDIODE\_0}{AREA} \tag{26}$$

$$RDIODE\_1 = \frac{RDIODE\_1}{AREA} \tag{27}$$

5. MET LDMOS Model Equations

5.1 The temperature dependency of parasitic resistances is given by:

$$Rg = RG\_0 + RG\_1 * (T - TNOM) \tag{28}$$

$$Rd = RD\_0 + RD\_1 * (T - TNOM) \tag{29}$$

$$Rs = RS\_0 + RS\_1 * (T - TNOM) \tag{30}$$

$$T = Vth\_rise + V\_tsnk + 273 = Vth\_rise + TSNK + 273 \tag{31}$$

where *T* is the actual or total temperature (not the temperature rise) in K and *TNOM* is the temperature at which the parameters were extracted. The value of *V_tsnk* (°C) is numerically equal to the heat sink temperature *TSNK* (°C). Notice that eventhough *RG_1*, *RD_1* and *RS_1* have units of Ω/K, their numerical value will be the same if the units are Ω/°C.

5.2 The forward bias drain to source current equation is given by:

$$Vto\_f = VTO\_0 + VTO\_1 * (T - TNOM) \tag{32}$$

$$Beta = BETA\_0 + BETA\_1 * (T - TNOM) \tag{33}$$

$$Vbr = VBR\_0 + VBR\_1 * (T - TNOM) \tag{34}$$

To maintain small signal to large signal model consistency, the gate to source voltage used in the calculation of the large signal drain to source current is delayed TAU seconds.

$$Vgs\_delayed(t) = Vgs(t - TAU) \tag{35}$$

$$Vgst2 = Vgs\_delayed - (Vto\_f + (GAMMA * Vds)) \tag{36}$$

$$Vgst1 = Vgst2 - \frac{1}{2}\left(Vgst2 + \sqrt{(Vgst2 - VK)^2 + DELTA^2} - \sqrt{VK^2 + DELTA^2}\right) \tag{37}$$

$$Vgst = VST * ln\left(e^{\frac{Vgst1}{VST}} + 1\right) \tag{38}$$

$$Vbreff = \frac{Vbr}{2}(1 + Tanh[M1 - Vgst * M2]) \tag{39}$$

$$Vbreff1 = \frac{1}{K2}(Vds - Vbreff) + M3\left(\frac{Vds}{Vbreff}\right) \tag{40}$$

$$Ids = (Beta)(Vgst^{VGEXP})(1 + LAMBDA * Vds)Tanh\left[\frac{Vds * ALPHA}{Vgst}\right](1 + K1 * e^{Vbreff1}) \tag{41}$$

5.3 The forward bias drain to source diode is given by:

$$Vt = \frac{k * T}{q} \tag{42}$$

where *k* is the Boltzmann's constant (1.381e-23 J/K), T is the temperature in Kelvin, and *q* is the electron charge (1.602E-19 C)

$$Idiode\_f = ISS\left(e^{\frac{(Vds - Vbr)}{N * Vt}}\right) \tag{43}$$

5.4 The reverse bias drain to source current equation is given by:

$$Vto\_r = VTO\_R + VTO\_1 * (T - TNOM) \tag{44}$$

$$Vgst2 = Vgs\_delayed - (Vto\_r - (GAMMA * Vds)) \tag{45}$$

$$Vgst1 = Vgst2 - \frac{1}{2}\left(Vgst2 + \sqrt{(Vgst2 - VK)^2 + DELTA^2} \right) - \sqrt{VK^2 + DELTA^2} \tag{46}$$

$$Vgst = VST * ln\left(e^{\frac{Vgst1}{VST}} + 1 \right) \tag{47}$$

$$Ids = (BR)(Vds)(Vgst) \tag{48}$$

5.5 The reverse bias drain to source diode is given by:

$$Vt2 = \frac{k * T}{q} \tag{49}$$

$$Ism = ISR * \left(\frac{T}{TNOM} \right)^{\frac{3}{NR}} e^{\left(\left(\frac{-Eg}{NR * Vt2} \right) * \left(1 - \frac{T}{TNOM} \right) \right)} \tag{50}$$

where *Eg* is the energy gap for Silicon which is equal to 1.11 [3] and T is temperature in Kelvin.

$$Idiode\_r = Ism * \left(e^{\frac{Vdiode\_r}{NR * Vt2}} - 1 \right) \tag{51}$$

The reverse diode's series resistance is given by:

$$Rdiode = RDIODE\_0 + RDIODE\_1 * (T - TNOM) \tag{52}$$

5.6 The gate to source capacitance equation is given by:

$$Cgs = \left(CGS1 + CGS2 * \left[1 + Tanh\left(CGS6 * (Vgs + CGS3) \right) \right] + CGS4 * \left[1 - Tanh\left(Vgs * CGS5 \right) \right] \right) * \left(1 + CGST * (T - TNOM) \right) \tag{53}$$

5.7 The gate to drain capacitance equation is given by:

$$Cgd = \left(CGD1 + \frac{CGD2}{1 + CGD3 * (Vgd - CGD4)^2} \right) * \left(1 + CGDT * (T - TNOM) \right) \tag{54}$$

5.8 The drain to source capacitance equation is given by:

$$Cds = \left(CDS1 + \frac{CDS2}{1 + CDS3 * Vds^2} \right) * \left(1 + CDST * (T - TNOM)\right) \tag{55}$$

5.9 The noise is calculated as shown in [3], as the sum of the thermal chanel noise and the flicker noise as shown by the following equation:

$$\overline{id^2} = \frac{8 * k * T * g_m}{3} + KF * \left(\frac{Ids^{AF}}{f^{FFE}} \right) \tag{56}$$

where g_m is the transconductance of the device at the operating point, T is temperature in Kelvin, and f is the frequency. In addition all resistors are also modeled as thermal noise sources.

$$\overline{id_R^2} = \frac{4 * k * T}{R} \tag{57}$$

where R is the resistance value and T is the temperature in Kelvin.

5.10 To avoid convergence problems the maximum temperature rise, Vth_rise (°C) is limited to 300 °C using the following equation:

$$Vth\_rise = \begin{cases} 0 & 0 \le Vth\_rise \\ Vth\_rise & 0 < Vth\_rise < 250 \\ 250 + 50 * tanh\left[\frac{Vth\_rise - 250}{50} \right] & 250 \le Vth\_rise \end{cases} \tag{58}$$

6. References

[1] W. Curtice, J. Plá, D. Bridges, T. Liang & E. Shumate, A New Dynamic Electro-Thermal Nonlinear Model for Silicon RF

LDMOS FETs, 1999 IEEE MTT-S International Microwave Symposium, Anaheim CA, pp. 419-422

[2] M. Golio, Microwave MESFETs and HEMTs, Arthec House, Boston, 1991, pp. 79-80

[3] P. Antognetti & G. Massobrio, Semiconductor Device Modeling with SPICE, McGraw Hill, New York, 1988.

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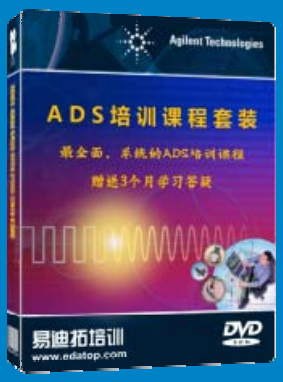

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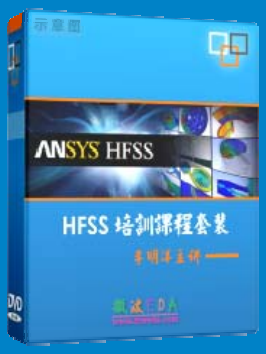

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