IPJ-W1510, IPJ-W1512, IPJ-W1513

Monza® 4 Tag Chip Datasheet

Overview

With the new **Monza**® 4 tag chips, Impinj builds upon the field-proven Monza chip family—well-regarded in the industry as the most reliable, consistent, flexible, and fully UHF Gen 2-compliant tag chips available. The Monza 4 family provides a variety of models to suit diverse applications, ushering in new standards in RFID privacy, tag orientation insensitivity, best and most consistent read/write performance, and memory capability.

Features

- **True3D™ antenna technology**—patented, dual-differential antenna ports enable compact omni-directional tags, improving item-level read reliability
- **QT™ technology**—protects business sensitive data while assuring consumers of privacy
  - **Private/Public** data profiles—two different memory maps that enable tag owners to control exposure of data
  - **Short-range** option to prevent unauthorized access
- Available memory options to support large user-memory applications
- **Block permalocking** adds flexibility in memory usage
- Custom S1 flag refresh facilitates inventory of hard-to-read tags
- Custom EPC+TID backscatter allows rapid tag authentication
- Superior read sensitivity of -17.4 dBm (single port operation) or -19.9 dBm (with True3D), combined with excellent interference rejection yields a read range of 16 meters (single port) or 21 meters (with True3D)
- Industry-leading write sensitivity of -14.6 dBm for unparalleled commissioning and bulk encoding reliability.
- Write rate of 5 ms for 32-bit writes enables 1200 tags/minute programming
- Extended temperature range (-40 ^{o}C to +85 ^{o}C) for reliable performance under hard conditions
- Impinj's field-rewritable NVM (optimized for RFID) provides 100,000-cycle/50-year retention reliability
- EPCglobal and ISO 18000-6C compliant

Table of Contents

1 Introduction

1.1 Scope

This datasheet defines the physical and logical specifications for Gen 2-compliant Monza 4 tag silicon, a reader-talks-first, radio frequency identification (RFID) component operating in the UHF frequency range.

1.2 Reference Documents

EPC™ Radio Frequency Identity Protocols Class-1 Generation-2 UHF RFID Protocol for Communications at 860 MHz – 960 MHz, Version 1.2.0 (Gen 2 Specification). The conventions used in the Gen 2 Specification (normative references, terms and definitions, symbols, abbreviated terms, and notation) were adopted in the drafting of this Monza 4 Tag Chip Datasheet. Users of this datasheet should familiarize themselves with the Gen 2 Specification.

Impinj Monza Wafer Assembly Specification

Impinj Monza Wafer Map Orientation

EPC™ Tag Data Standards Specification

EPCglobal "Interoperability Test System for EPC Compliant Class-1 Generation-2 UHF RFID Devices" v.1.2.4, August 4, 2006. (Monza 4 tag chips are compliant with this Gen 2 interoperability standard.)

2 Functional Description

The Monza 4 tag chip family fully supports all requirements of the Gen 2 specification as well as many optional commands and features (see Section 2.5 below). In addition, the Monza tag chip family introduces a number of enhancements over current chips on the market:

- Superior sensitivity yields highly improved performance, read/write range/reliability, and write rate
- Impinj patented True3D™ antenna technology enables smaller, less expensive tags with better performance, and supports orientation insensitivity without compromised performance
- Impinj patented QT™ technology provides additional options for data protection, giving the user the ability control access to business-sensitive data
- Increased memory size options and in some models, the ability to permanently lock individual blocks of memory provide added flexibility
- Custom, yet fully Gen 2 compliant S1 flag refresh and EPC + TID backscatter modes add more capability for previously difficult tagging applications

2.1 True3D Antenna Technology Improves Performance

The Monza 4 tag chip has an architecture unlike any other chip on the market. With True3D antenna technology, two fully independent, differential inputs enable omni-directional antenna designs, eliminating orientation-related missed reads or blind spots. (See section 3.1 for details about how to connect to these inputs.) Orientation insensitivity is particularly important in item-level applications and in situations where handheld readers are the norm.

For item-level tags, variability in orientation can be too great to overcome easily. For example, in a retail apparel application, the variety of ways an RFID tag on a garment might lay with respect to a reader are endless: folded on a shelf, hanging on a rack, boxed in the backroom, crumpled on the floor in the changing room, etc. To expect this tag to always have a particular orientation that facilitates reading is not realistic. In such cases, true omni-directional tag designs are paramount to successful data capture.

With the new Monza 4 tag chip architecture, this type of orientation indifference is possible. To illustrate the difference between conventional tag chips and the Monza 4, examining their read range responses is useful.

Figure 2-2 provides a read range response plot for a conventional single-port tag using a dipole antenna configuration. Any single port tag, even using the best chip and innovative antenna design, will have a deficiency somewhere in its pattern. While the tag depicted in Figure 2-1 has excellent broadside performance, there are certain angles where a tag is less visible to a reader.

With the previous generation Monza tag chip, clever antenna design that took advantage of its dual input structure helped to remove the blind spots, or nulls (see Figure 2-2), but came at the cost of a compromise in long-range performance.

Figure 2-3 provides a read range response pattern for a tag using a Monza 4 tag chip. Compare Figure 2-3 to Figure 2-2. Notice that the response patterns in the Monza 4-based tag (Figure 2-3) are close to circular—no angle has significantly lower sensitivity than any other. And at every angle, the read range has increased.

With Monza 4 and True3D antenna technology, users achieve orientation insensitivity as well as excellent performance.

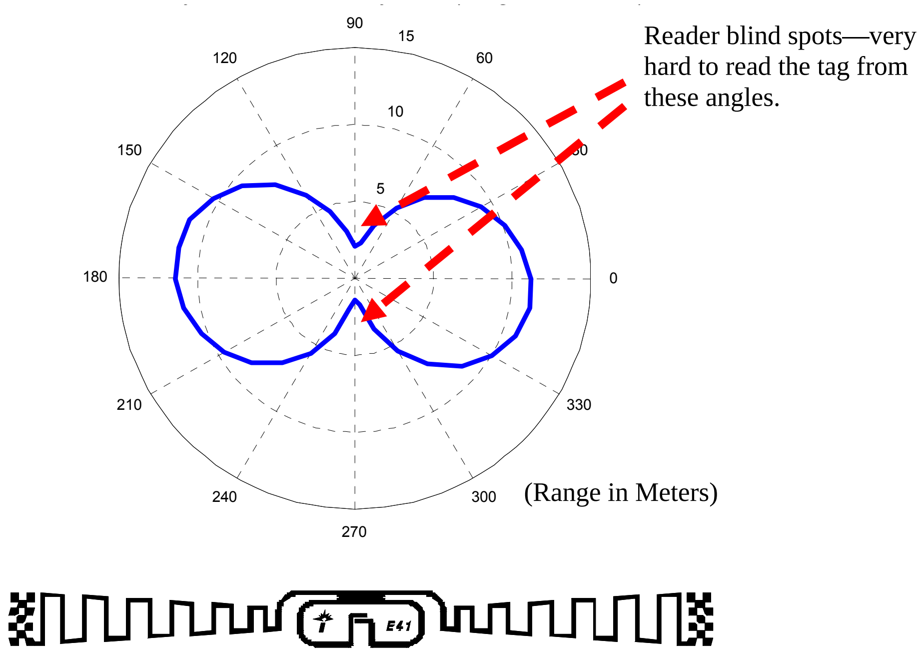


Figure 2-1 Read Range Response for Monza 4 on a 95 x 8 mm Dipole Antenna

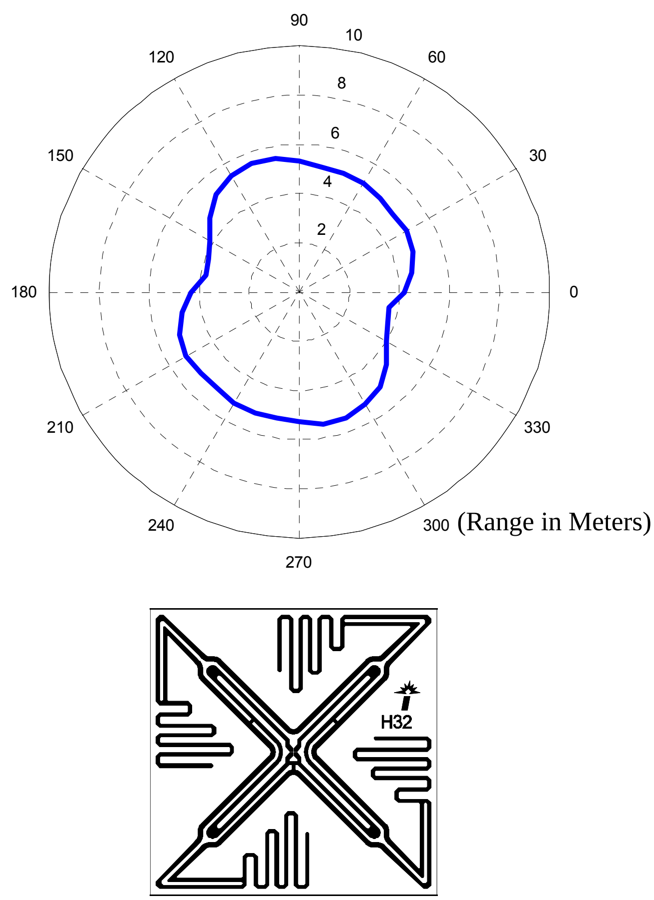
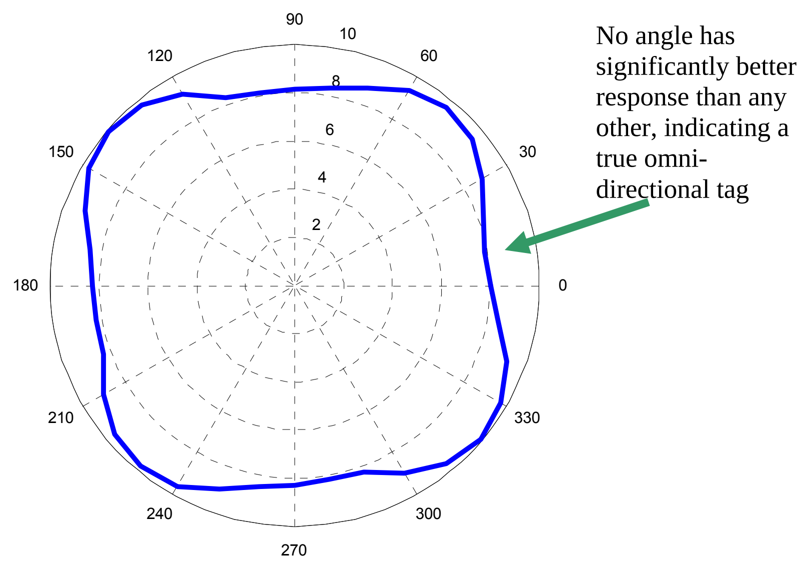


Figure 2-2 Read Response for Monza 3-Based, 46 mm^2 Tag (Impinj H32)



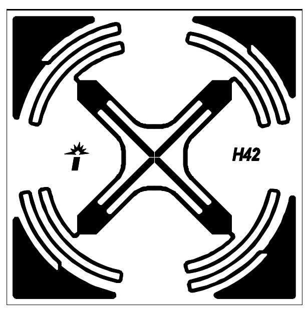


Figure 2-3 Monza 4-Based, 46 mm^2 Tag (Impinj H42) Provides Orientation Insensitivity *and* Excellent Performance by utilizing True3D Antenna Technology

2.2 QT Technology–Private, Public, Peek, and Short Range

Through QT technology, a tag owner/user can maintain two data profiles (one public, one private), allowing confidentiality of business-sensitive data while assuring consumers of privacy. The tag owner stores confidential data in the private data profile, which is protected by a password-controlled command and may only be accessed at very short read distances.

One example where such a feature would be useful is in a supply chain for luxury goods. The manufacturer may want to include information in the tag that would provide a guarantee of authenticity, record the time and place of manufacture for guarantee purposes, or include serial numbers.

After that item is packaged for distribution, however, such details might provide a security risk. If anyone possessing a reader can determine details about what is in a particular box, high-value goods could get diverted.

The Monza 4 tag chip's unique set of features helps to solve this problem.

2.2.1 Private/Public Profiles

The **Private/Public** profile capability, available in Monza 4QT tag chips, provides two memory configurations (i.e., profiles) in a single chip—one **Private** and one **Public**. A Monza 4QT chip only exposes a single profile at a time. Figure 2-4 shows the chip's memory configuration when in the **Private** profile. The EPC memory typically contains an item serial number. The User memory might hold detailed information about the item. The TID memory, which includes a 32 bit base TID, a 16 bit extended TID header, and a 48 bit serial number, uniquely identifies the Monza 4QT chip itself. Also included in TID memory is a 96 bit Public EPC, which is field-writeable by a user. In typical applications, the user writes a Public EPC value into this memory location then “publicizes” the tag. Although users are free to encode as little or as much information into this 96 bit Public EPC field as they chose (including no information at all), Impinj recommends certain usage guidelines to prevent these 96 bit Public EPCs from colliding with other tags. See section 2.2.5 for Impinj’s recommended usage guidelines.

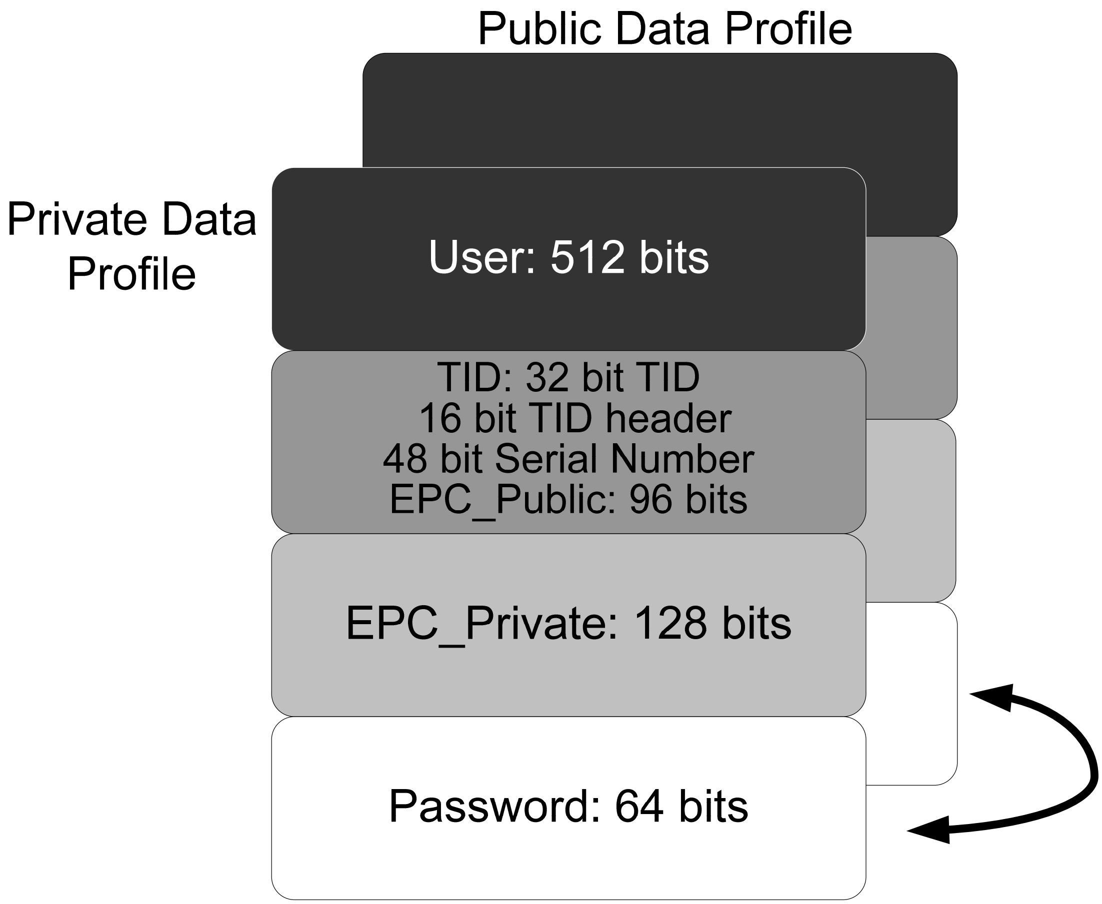


Figure 2-4 Monza 4QT Tag Chip Private Data Profile

At any point in the supply chain, for example at point-of-sale, users have the ability to switch QT tags to the **Public** profile. Figure 2-5 illustrates this profile. Once switched, the tag conceals its 128 bit EPC (EPC_Private), User Memory, 16 bit TID header, and 48 bit serial number. The tag exposes its Public EPC in EPC memory, remapped from its prior location in TID memory. When the tag is singulated, it sends this 96 bit public EPC. The only other information available to a reader is the 32 bit base TID. All other private memory contents appear non-existent to a reader reading the tag.

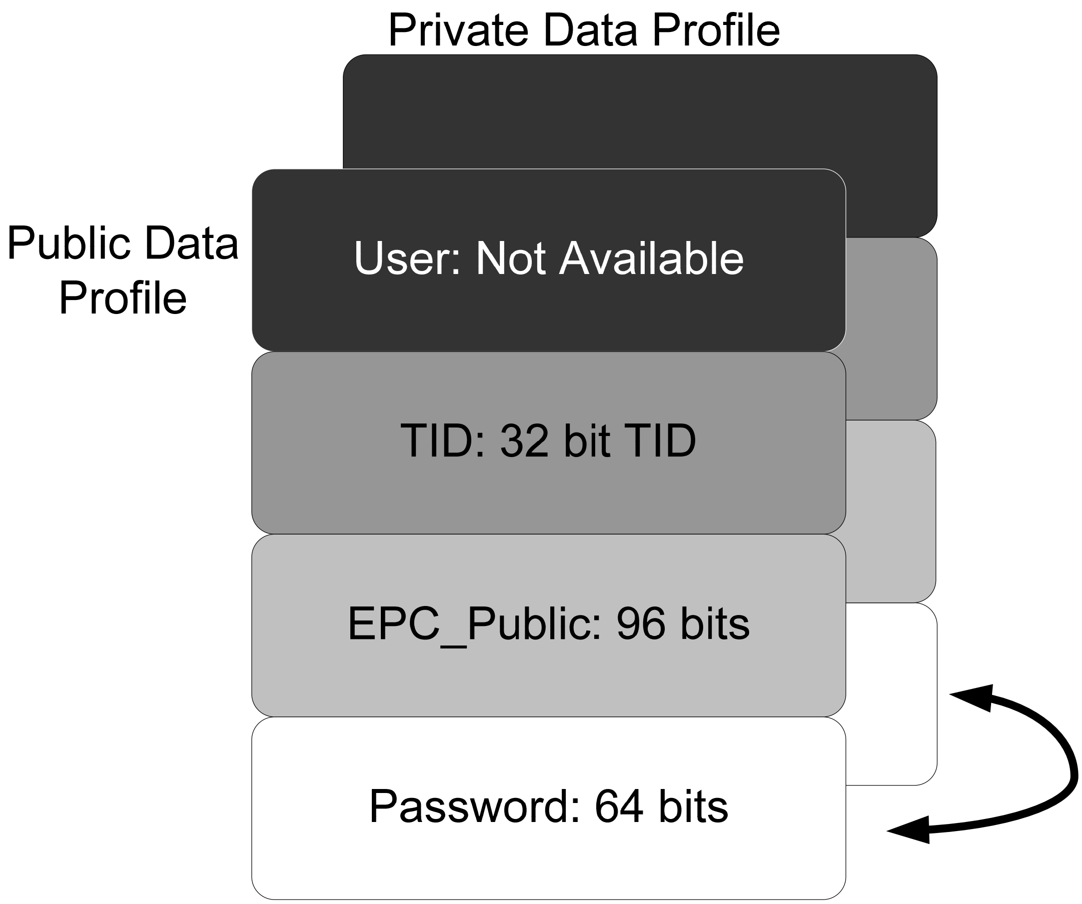


Figure 2-5 Monza 4QT Tag Chip Public Data Profile

The Private/Public profile features of the Monza 4QT tag chip are controlled by the QT command. Tags may be switched from Private profile to Public profile and back again, using the QT command. This QT command can be protected by a Short-Range Feature, by the tag's access password, or by both. See 2.2.2.

2.2.2 Public/Private Profile Protection

To secure the Private profile tag data, Monza 4QT chips offer a **Short-Range** feature. The Short-Range feature adds a layer of physical security by preventing readers farther than roughly one meter from the tag from switching the tag from Public to Private (or vice versa).

When Short Range is enabled, the tag reduces its sensitivity in the OPEN and SECURED states by about 15 dB. The tag has normal sensitivity during singulation. However, before transitioning to the OPEN or SECURED states, the tag checks the RF power level—if it is above the short-range threshold then the tag will enter the OPEN or SECURED state, otherwise the tag will reset back to the READY state. The QT command is only available when a tag is in the SECURED state, so this power check effectively prevents the tag from accepting a QT command at long range.

A reader is always able to read a tag's currently exposed EPC (EPC_Public or EPC_Private, as appropriate for the current profile) at maximum range. However, when the Short-Range feature is enabled, a reader at long range that attempts to switch the tag's profile (for example, from Public to Private to read the tag's User memory) will see the tag lose power and drop out of its dialog with the reader. This short-range feature ensures that the information the tag's rightful owner wants to protect is not readable unless the tag is close to a reader antenna.

As a further layer of protection, the Access command defined in the Gen 2 specification is fully operable for QT-enabled tags. If the tag's Access password is nonzero, a reader must provide this password before the tag will transition to the SECURED state. Because the QT command is only operable from the SECURED state, the Access password provides a secure mechanism against unauthorized readers issuing a QT command. In short, a QT tag can use physical protection (Short Range), logical protection (Access password) or both to prevent unauthorized access.

The Short Range feature is controlled by the QT command. (See Table 2-1 through Table 2-3.) The specific bit that controls the Short Range mode is the QT_SR bit described in Table 2-3.

2.2.3 Peek

What would happen if a Public tag is switched to Private by an authorized user, for example to read User memory, and inadvertently left in the Private mode? In this situation, the tag could compromise its Private data. To help prevent this situation, Monza 4QT tag chips offer a **Peek** feature. With Peek, a reader can temporarily switch a Public tag to Private, access the Private information, then when the chip loses power it will automatically revert to its Public profile. Peek is controlled by the persistence bit in the QT command—to implement a Peek, set the Persistence bit to 0 in the QT command. See Table 2-2 for details.

2.2.4 QT Command Format

Table 2-1, Table 2-2, and Table 2-3 provide details about the custom Impinj QT command.

Table 2-1 QT Command Code

Command	Code	Length (bits)	Details
QT	1110000000000000	68	• The QT command controls the switching of Monza 4QT between the Private and Public profiles • The tag must be in the SECURED state to transition to the memory indicated by the command • If a tag receives a QT command with an invalid handle, it ignores that command • The tag responds with the Insufficient Power error code if the power check fails on write • The tag responds with the Other error code if the write times out

Table 2-2 QT Command Details

QT Command	Code	Read/Write	Persistence	RFU	Payload	RN	CRC-16
#bits	16	1	1	2	16	16	16
Details	1110000000000000	0: Read 1: Write	0: Temporary 1: Permanent	00_b	QT Control	handle	

Table 2-3 QT Command Field Descriptions

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>Read/Write</td><td>The Read/Write field indicates whether the tag reads or writes QT control data.
Read/Write=0 means read the QT control bits in cache.
Read/Write=1 means write the QT control bits</td></tr>
<tr><td>Persistence</td><td>If Read/Write=1, the Persistence field indicates whether the QT control is written to nonvolatile (NVM) or volatile memory.
Persistence=0 means write to volatile memory.
Persistence=1 means write to NVM memory</td></tr>
<tr><td>RFU</td><td>These bits are reserved for future use and will be ignored by Monza 4</td></tr>
<tr><td>Payload</td><td>This field controls the QT functionality. These bits are ignored when the Read/Write field equals 0.
Bit 15 (MSB) is first transmitted bit of the payload field.
<table>
<tr><th>Bit #</th><th>Name</th><th>Description</th></tr>
<tr><td>15</td><td>QT_SR</td><td>1: Tag reduces range if in or about to be in OPEN or SECURED state
0: Tag does not reduce range</td></tr>
<tr><td>14</td><td>QT_MEM</td><td>1: Tag uses Public Memory Map (see Table 2-10)
0: Tag uses Private Memory Map (see Table 2-9)</td></tr>
<tr><td>13:0</td><td colspan="2">Reserved for future use. Tag will return these bits as zero.</td></tr>
</table></td></tr>
<tr><td>RN</td><td>The tag will ignore any QT command received with an invalid handle</td></tr>
</table>

The tag response to the QT Command with Read/Write = 0 uses the preamble specified by the TRext value in the Query command that initiated the round. See Table 2-4 for read response details.

Table 2-4 Tag Response to QT Read Command

	Header	Data	RN	CRC-16
#bits	1	16	16	16
Description	0	RFS Control	handle	

The tag response to the QT Command with Read/Write =1 uses the extended preamble. See Table 2-5 for write response details. Note that a reader should not presume that a tag has properly executed a QT Write command unless and until it receives the response shown in Table 2-5 from the tag.

Table 2-5 Tag Response to a Successful QT Write Command

	Header	RN	CRC-16
#bits	1	16	16
Description	0	Handle	

2.2.5 Recommended Public EPC Usage Guidelines

The EPCglobal Tag Data Standards specifies the general structure of the EPC data field (for the latest version of this standard, visit www.epcglobalinc.org). If tag users wish to have the Public EPC hold information in any of the currently defined formats (e.g., SGTIN-96), they should follow this specification.

For any other use of this data field, tag users must take care not to create content that conflicts with the standard. For example, a retailer should not set the MSBs to “0011 0000” because that could be interpreted as an SGTIN-96-tagged item.

To create Public EPCs that do not conflict with already defined usage, Impinj recommends the following (also see Table 2-6):

- The first 8 bits of header should always be zero to avoid conflict with already standardized EPC formats.
- The next 32 bits should hold a Private Enterprise Number (PEN) (number obtainable from the Internet Assigned Numbers Authority (IANA) at http://pen.iana.org/pen/app) that uniquely identifies a company or organization. If tag users do not wish to have even this level of identification (i.e., they desire full privacy), the PEN should be set to all zeros.
- The last 56 bits hold data fields specified by each entity for their application.

Table 2-6 Recommended Format for Public EPC Contents

Header (00000000)	Private Enterprise Number (32 bits)	Data Fields (56 bits)

2.2.5.1 Example Public EPC Use Case—Retail Environment

After a sale, a retailer might conceal any proprietary information available in the EPC_Private memory by switching the tag to the Public profile. But they still need a means of verifying that a particular item came from their company to support return logistics. And to avoid consumer privacy concerns, any information entered into the EPC_Public memory must not be unique.

By setting up a format such as that shown in Table 2-7, the retailer has sufficient information to support returns, verify that the item came from their company, determine the type of return, and identify stolen merchandise without having such unique numbers that a consumer’s privacy is at risk.

Note: This format is for illustration purposes only. Tag users should consult the EPC Tag Data Standard when designing their format to ensure compliance.

Table 2-7 Example EPC_Public Format—Retail Case

Header (8 bits)	PEN (32 bits)	Mode (8 bits)	Store Number (16 bits)	Date Code (32 bits)	Comment
00_h	$0000\ 0000_h$	00_h	0000_h	$0000\ 0000_h$	Full Privacy Mode
00_h	$0000\ 0192_h$	01_h	$000F_h$	$00C1\ F7DA_h$	Store Return
00_h	$0000\ 0192_h$	02_h	$000F_h$	$00A1\ 07DA_h$	Store Return, Password Required
00_h	$0000\ 0192_h$	03_h	$000F_h$	$FFFF\ FFFA_h$	Date Field Coded to Indicate that Item Was Not Sold

2.3 Increased Memory Options

Tag users have asked for increased memory in RFID tag chips, and the Monza 4 family offers a variety of options. See Table 2-8. For detailed memory maps, see Section 4 below. The extended User memory option supports applications where users cannot count on a database connection. The 512 bits of User memory enables a portable, but private database to travel with the tag. The Extended EPC memory option enables compliance with regional and industry-segment mandates that require more than 96 bit EPC numbers, as well as provides a faster access form of memory.

Table 2-8 Monza 4 Memory Options

Model	User Memory	EPC Memory	True3D Antenna Technology	Serialized TID	QT technology
Monza 4QT	512	128[1]	✓	✓	✓
Monza 4E	128	496[1]	✓	✓	–
Monza 4D	32	128[1]	✓	✓	–

Note 1: Programmed to 96 bits out of factory.

2.3.1 Extended User Memory Option

Impinj offers a version of Monza 4 (Monza 4QT) with 512 bits of user memory, 128 bits of EPC memory, and a serialized TID. See Table 2-9.

In addition to the increased memory size, Monza 4QT tag chips offer the ability to independently lock four fixed, 128-bit sections of user memory (block permalock). This feature is particularly useful for situations such as in a supply chain, where various participants along the chain may want to record data, but not necessarily have it be openly available to all parties.

Table 2-9 Monza 4QT (Private Mode) Memory Organization

Memory Section	Description
User	512 bits
TID (not changeable)	Serial Number—48 bits
	Extended TID Header—16 bits
	Company/Model Number—32 bits
EPC_Public	96 bits
EPC_Private	128 bits
Passwords	Kill/Access—64 bits

Table 2-10 Monza 4QT (Public Mode) Memory Organization

Memory Section	Description
TID (not changeable)	Company/Model Number—32 bits
EPC_Public	96 bits
Passwords	Kill/Access—64 bits

2.3.2 Extended EPC Memory Option

Because of the way the protocol works, data stored in user memory requires multiple steps to access. For situations where memory must be accessed with some degree of speed, a larger User memory may not meet access speed requirements. To provide larger memory with the type of throughput required by some applications as well as meet the needs of applications requiring greater than 96 bit EPC numbers, Impinj also offers a variant of the Monza 4 tag chip with increased EPC memory. See Table 2-11.

Table 2-11 Monza 4E Memory Organization

Memory Section	Description
User	128 bits
TID (not changeable)	Serial Number—48 bits
	Extended TID Header—16 bits
	Company/Model Number—32 bits
EPC	496 bits
Passwords	Kill/Access—64 bits

2.3.3 Basic Memory Option

For applications where large memory is not required, the Monza 4D offers the superior sensitivity, True3D antenna support and unique TID with a more standard memory size. See Table 2-12.

Table 2-12 Monza 4D Memory Organization

Memory Section	Description
User	32 bits
TID (not changeable)	Serial Number—48 bits
	Extended TID Header—16 bits
	Company/Model Number—32 bits
EPC	128 bits
Passwords	Kill/Access—64 bits

2.4 Supporting Difficult-to-Read Tags and Fast Serial Number Access

The Monza 4 tag chip family offers a feature unique to Impinj, called S1 flag refresh. This fully UHF Gen 2 compliant feature enables a reader to instruct an Impinj tag to continue to refresh its A/B flag setting such that it remains in a non-responsive state. By instructing tags that have already been inventoried to remain unresponsive while searching for tags not yet inventoried, the reader has a far greater chance of finding difficult-to-read tags.

Monza 4QT (in Private profile mode) tag chips also support a feature which will result in the backscatter of both the EPC and the TID (containing the serial number) information upon command. This feature improves throughput in applications where TID information is required.

2.5 Support for Optional Gen 2 Commands

Monza 4 tag chips support the optional commands listed in Table 2-13.

Table 2-13 Supported Optional Gen 2 Specification Commands

Command	Code	Length (bits)	Details
Access	11000110	56	
BlockWrite	11000111	>57	• Accepts valid one-word commands • Accepts valid two-word commands if pointer is an even value • Returns error code (00000000_2) if it receives a valid two-word command with an odd value pointer • Returns error code (00000000_2) if it receives a command for more than two words • Does not respond to block write commands of zero words
BlockPermalock	11001001	>66	• User Memory in Monza 4QT (in Private mode) versions only • Four blocks, each 128 bits in size • Ignored by Monza 4E, Monza 4D, and Monza 4QT (in Public mode)

2.6 Monza 4 Tag Chip Block Diagram

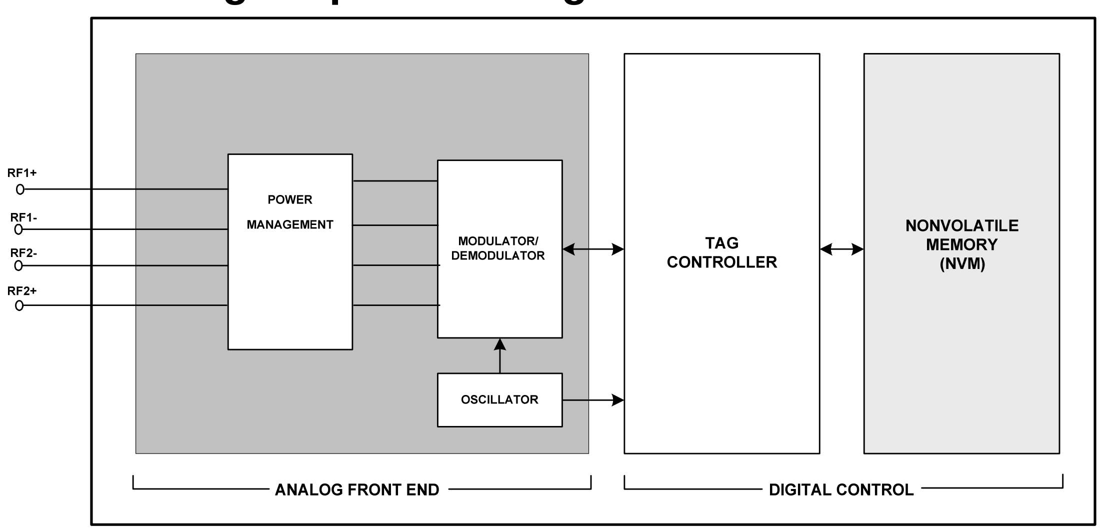


Figure 2-6 Block Diagram

2.7 Pad Descriptions

Monza 4 tag chips have four external pads available to the user: RF1+, RF1-, RF2+, and RF2-, which are two fully independent, differential antenna ports (with one positive and one negative input pad each), as shown in Table 2-14 (see also Figure 2-6, and Figure 2-7). Note that none of these pads connects to the chip substrate.

Table 2-14 Pad Descriptions

External Signals	External Pad	Description
RF1+	1	Differential RF Input Pads for Antenna 1, which are isolated from the RF Input Pads for Antenna 2
RF1-	1	
RF2+	1	Differential RF Input Pads for Antenna 2, which are isolated from the RF Input Pads for Antenna 1
RF2-	1	

2.8 Dual Antenna Input

All interaction with the Monza 4 tag chip, including generation of its internal power, air interface, negotiation sequences, and command execution, occurs via its two differential antenna ports. The dual antenna ports enable antenna design diversity, which in turn minimizes a tag's orientation sensitivity, particularly when the two antennas are of different types (e.g., a combination of loop and dipole) or are otherwise oriented on different axes (X-Y). The dual antenna port configuration also enables increased read and write ranges.

The two antenna ports operate independently. The power management circuitry receives power from the electromagnetic field induced in the pair, and the demodulator exploits the independent antenna connections, combining the two demodulated antenna signals for processing on-chip.

Monza 4 tag chips may also be configured to operate using a single antenna port by simply connecting just one of the two antenna ports. The unused port should be left to float.

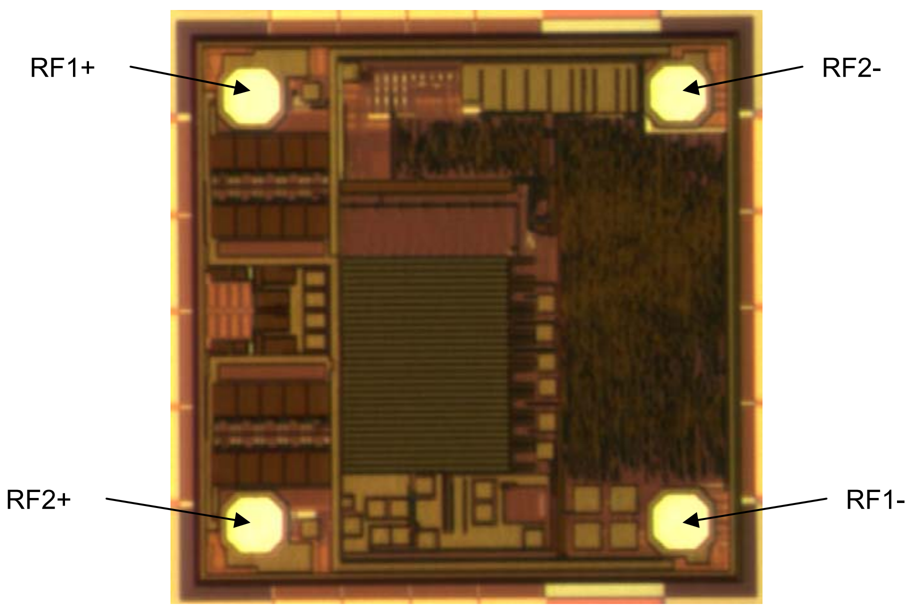


Figure 2-7 Monza 4 tag chip die orientation

2.9 Power Management

The tag is activated by proximity to an active reader. When the tag enters a reader's RF field, the Power Management block converts the induced electromagnetic field to the DC voltage that powers the chip.

2.10 Modulator/Demodulator

The Monza 4 tag chip demodulates any of a reader's three possible modulation formats, DSB-ASK, SSB-ASK, or PR-ASK with PIE encoding. The tag communicates to a reader via backscatter of the incident RF waveform by switching the reflection coefficient of its antenna pair between reflective and absorptive states. Backscattered data is encoded as either FM0 or Miller subcarrier modulation (with the reader commanding both the encoding choice and the data rate).

2.11 Tag Controller

The Tag Controller block is a finite state machine (digital logic) that carries out command sequences and also performs a number of overhead duties.

2.12 Nonvolatile Memory

Monza 4 tag chip embedded memory is nonvolatile memory (NVM) cell technology, specifically optimized for exceptionally high performance in RFID applications. All programming overhead circuitry is integrated on chip. Monza 4 tag chip NVM provides 100,000 cycle endurance/ 50-year data retention.

The NVM block is organized into three segments:

- User memory (32, 128, or 512 bits depending on model)
- EPC Memory (128 or 496 bits, depending on model)
- Reserved Memory (which contains the Kill and Access passwords).

The ROM-based Tag Identification (TID) memory contains the EPCglobal class ID, the manufacturer identification, and the model number. For Monza 4, it also contains an extended TID consisting of a 16-bit header and 48-bit serialization.

3 Interface Characteristics

This section describes the RF interface of the tag chip and the modulation characteristics of both communication links: reader-to-tag (Forward Link) and tag-to-reader (Reverse Link).

3.1 Making Connections

The Monza 4 family of tag chips takes advantage of Impinj's patented rectifier technology to implement dual, independent ports. A port is defined between a pair of pads: the RF1+ and RF1- pair together forming Port 1 and the RF2+ and RF2- pair forming Port 2. A conceptual diagram of the RF front-end is shown in Figure 3-1. The two ports have identical electrical properties. See Section 3.1.4 for the target source impedance recommended by Impinj for best operation.

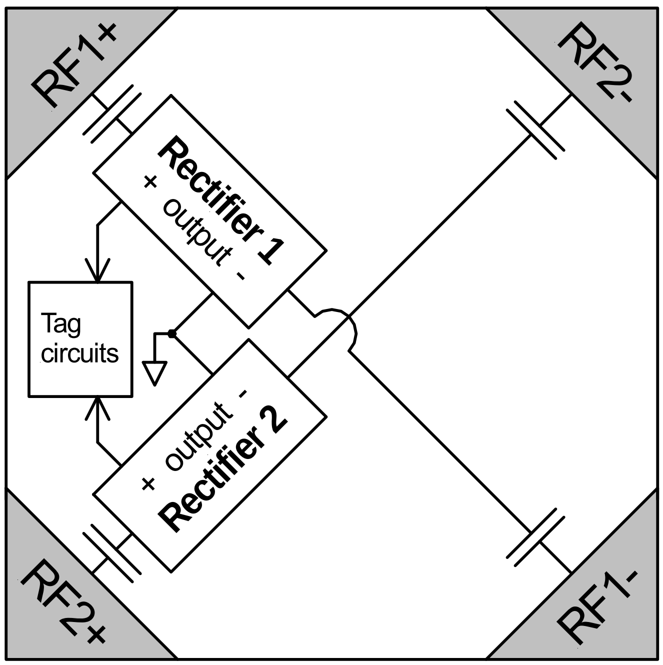


Figure 3-1 Conceptual model of dual independent ports

3.1.1 Single-port Connection Option

In the single-port configuration, the signal is applied to just one of the Monza 4 antenna ports. The antenna connects to a diagonal pair of pads and the remaining, unused pads are electrically isolated from the active traces. Figure 3-2 shows two examples of Impinj near-field antennas (Button and Blade) designed for connection in this fashion. The single-port configuration is common for near-field tag antennas and for very small or very thin antennas. It is not possible, however, to achieve true orientation insensitivity with a single port.

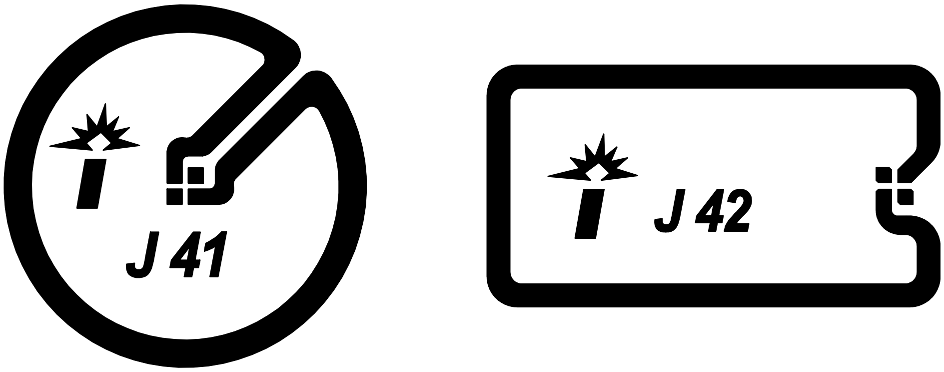


Figure 3-2 Antennas designed for a single-port connection. Button antenna (Left) and Blade antenna (Right), with antenna trace connections to diagonal pads of Monza 4.

The single-port configuration allows the chip to be mounted to the antenna at any 90 degree increment of rotation, as all four possible placements produce a valid connection between the antenna terminals and one of the Monza 4 ports. Because the two ports are electrically identical, there is no preferred orientation. The valid connections are shown in Figure 3-3, where the pad locations filled in black are those that are connected to the antenna traces. The dashed lines represent the electrical connections within the chip. For contrast, the figure also illustrates an adjacent pad connection, which is acceptable for some Impinj tag chips but not for Monza 4.

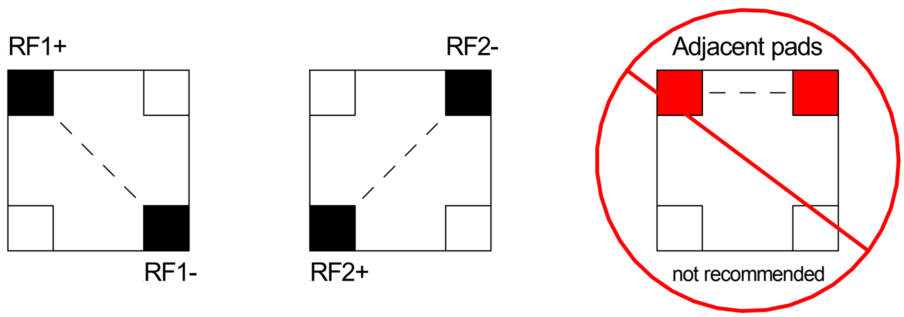


Figure 3-3 Chip/antenna connection possibilities for single-port configuration

3.1.2 Shunted-port Connection Option

In some rare circumstances, the antenna designer may find benefit in having a higher input capacitance. One example is in the design of very small, near-field antennas. The standard single-port connection presents a capacitance that resonates with a loop of approximately 12 mm diameter in a near-field tag such as the Button. If an application calls for a smaller tag, it is possible to employ the shunted-port connection to increase the input capacitance and reduce the loop size. This configuration, illustrated in Figure 3-4, energizes both ports simultaneously and loads the antenna with approximately twice the capacitance of a single port. A conductor loop with a diameter of about 7 to 8 mm is resonant with the shunted-port capacitance. This configuration incurs a slight (0.5 dB) efficiency penalty with corresponding loss in sensitivity compared to the single-port configuration, so it should be reserved for situations that mandate a very small tag.

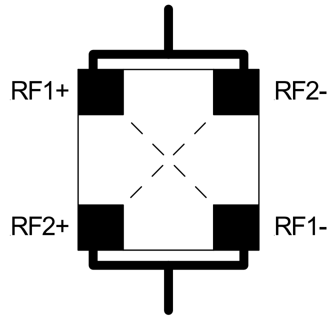


Figure 3-4 Chip/antenna connection for shunted-port configuration

3.1.3 Dual-port Connection Option

The advanced capabilities of Monza 4 really shine with a dual-port connection. This configuration is the focus of the True3D technology that enables high-readability, orientation-insensitive tags. One of the fundamental principles for achieving such high levels of performance is *symmetry by design*. The ports of Monza 4 have an inherent electrical symmetry along both diagonal axes of the chip. A good antenna that extends that symmetry out to a larger geometry and into its resonant modes is ideal for realizing True3D. An example of geometry that exhibits symmetry by design is shown in Figure 3-5.

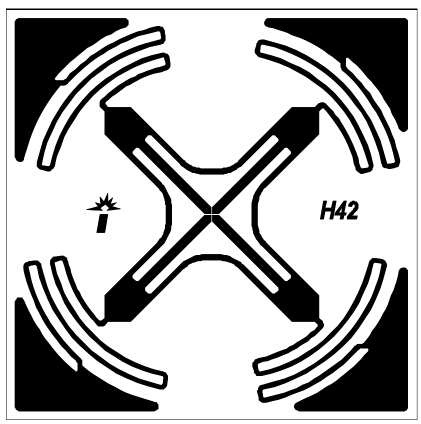


Figure 3-5 Antenna design for dual-port connection. The geometry is formed by rotating and copying a one-quadrant "primitive," resulting in rotational symmetry.

Symmetry in design leads to an electrical symmetry that minimizes the interaction between the two ports. Therefore, the antenna impedance at one port is independent of the load on the other port, and the design can proceed in a straightforward manner using the single-port antenna impedance recommendations. These recommendations are applied across one of the diagonal pairs of antenna pads and are guaranteed by design to apply to the other pair.

3.1.4 Source Impedance

Table 3-1 shows the chip port impedances for Monza 4 tag chips across center frequencies of the primary regions of operation (North America, Europe, and Japan) for the single port configuration.

Table 3-1 Chip Port Impedances

Parameter		Typical Value	Comments
Intrinsic Capacitance[1]		1000 fF	Measured on bare die between pads RF1+ and RF1-, or between pads RF2+ and RF2-
Single-port connection			
Chip Load Model		1650 Ω || 1.21 pF	Linearized model of chip port, including typical mounting capacitance
Conjugate Match Impedance	866 MHz	13 + j151 Ω	Complex conjugate of Chip Load Model at specified frequency, expressed as an impedance
	915 MHz	11 + j143 Ω	
	956 MHz	10 + j137 Ω	
Read Sensitivity		-17.4 dBm	Measured at 25 °C; R=>T link using DSB-ASK modulation with 90% modulation depth, Tari=25 µs, and a T=>R link operating at 256 kbps with Miller M=4 encoding.
Write Sensitivity		-14.6 dBm	
Shunted-port connection			
Chip Load Model		1000 Ω || 2.48 pF	Linearized model of chip port, including typical mounting capacitance
Conjugate Match Impedance	866 MHz	5.5 + j74 Ω	Complex conjugate of Chip Load Model at specified frequency, expressed as impedance. For near field-only tag, disregard real component.
	915 MHz	4.9 + j70 Ω	
	956 MHz	4.5 + j67 Ω	
Read Sensitivity		-16.9 dBm	Measured at 25 °C; R=>T link using DSB-ASK modulation with 90% modulation depth, Tari=25 µs, and a T=>R link operating at 256 kbps with Miller M=4 encoding
Write Sensitivity		-14.1 dBm	
Dual-port connection			
Chip Load Model		1800 Ω || 1.21 pF	Ports act independently, so each port of a dual-port tag has the same impedance parameters as a single-port tag
Read Sensitivity		-19.9 dBm	Power incident at each port under conditions of equal power, arbitrary phase relation between signals
Write Sensitivity		-17.1 dBm	

Note 1: Value does not include parasitic capacitance resulting from mounting the chip onto an antenna trace. Mounting capacitance is dependent on assembly parameters and manufacturing tolerance—users should evaluate and determine the appropriate mounting capacitance for their given process.

3.2 Reader-to-Tag (Forward Link) Signal Characteristics

Table 3-2 Forward Link Signal Parameters

Parameter	Minimum	Typical	Maximum	Units	Comments
RF Characteristics					
Carrier Frequency	860		960	MHz	North America: 902–928 MHz Europe: 865–868 MHz
Maximum RF Field Strength			+20	dBm	Received by a tag with dipole antenna while sitting on a maximum power reader antenna
Short Range Sensitivity		6.0 dBm			
Tag Velocity During 5ms Write			4.5 meters/sec		Under worst case fading conditions
Modulation Characteristics					
Modulation		DSB-ASK, SSB-ASK, or PR-ASK			Double and single sideband amplitude shift keying; phase-reversal amplitude shift keying
Data Encoding		PIE			Pulse-interval encoding
Modulation Depth (A-B)/A	80		100	%	
Ripple, Peak-to-Peak M_h=M_l			5	%	Portion of A-B
Rise Time ($t_{r,10\text{-}90\%}$)	0		0.33Tari	sec	
Fall Time ($t_{f,10\text{-}90\%}$)	0		0.33Tari	sec	
Tari[1]	6.25		25	µs	Data 0 symbol period
PIE Symbol Ratio	1.5:1		2:1		Data 1 symbol duration relative to Data 0
Duty Cycle	48		82.3	%	Ratio of data symbol high time to total symbol time
Pulse Width	MAX(0.265Tari,2)		0.525Tari	µs	Pulse width defined as the low modulation time (50% amplitude)

Note 1: Values are nominal; they do not include reader clock frequency error.

3.3 Reverse Link Signal Characteristics

Table 3-3 Reverse Link Signal Parameters

Parameter	Minimum	Typical	Maximum	Units	Comments
Modulation Characteristics					
Modulation		ASK			FET Modulator
Data Encoding		Baseband FM0 or Miller Subcarrier			
Change in Modulator Reflection Coefficient $\|\Delta\Gamma\|$ due to Modulation		0.8			$\|\Delta\Gamma\| = \|\Gamma_{reflect} - \Gamma_{absorb}\|$ (per read/write sensitivity, Table 3-2)
Duty Cycle	45	50	55	%	
Symbol Period[1]	1.5625		25	µs	Baseband FM0
	3.125		200	µs	Miller-modulated subcarrier
Miller Subcarrier Frequency[1]	40		640	kHz	

Note 1: Values are nominal minimum and nominal maximum, and do not include frequency tolerance. Apply appropriate frequency tolerance to arrive at absolute durations and frequencies.

4 Tag Memory

4.1 Monza 4 Tag Chip Memory Maps

Table 4-1 through Table 4-4 describe the memory maps for Monza 4QT (both the Private and Public modes), Monza 4E, and Monza 4D.

Table 4-1 Physical/Logical Memory Map–Monza 4QT (Private Mode)

Memory Bank Number	Memory Bank Name	Memory Bank Bit Address	Bit Number															
			15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
11_2	User (NVM)	$1F0_h$-$1FF_h$	**User[15:0]**															
		$1E0_h$-$1EF_h$	**User[31:16]**															
		…	**…**															
		10_h-$1F_h$	**User[495:480]**															
		00_h-$0F_h$	**User[511:496]**															
10_2	EPC_Public (NVM)	$B0_h$-BF_h	**EPC_Public [15:0]**															
		$A0_h$-AF_h	**EPC_Public [31:16]**															
		90_h-$9F_h$	**EPC_Public [47:32]**															
		80_h-$8F_h$	**EPC_Public [63:48]**															
		70_h-$7F_h$	**EPC_Public [79:64]**															
		60_h-$6F_h$	**EPC_Public [95:80]**															
	TID (ROM)	50_h-$5F_h$	**TID_Serial[15:0]**															
		40_h-$4F_h$	**TID_Serial[31:16]**															
		30_h-$3F_h$	**TID_Serial[47:32]**															
		20_h-$2F_h$	**Extended TID Header**															
		10_h-$1F_h$	Manufacturer ID				**Model Number**											
		00_h-$0F_h$	1	1	1	0	0	0	1	0	**Manufacturer ID**							
01_2	EPC_Private (NVM)	90_h-$9F_h$	**EPC_Private[15:0]**															
		80_h-$8F_h$	**EPC_Private [31:16]**															
		70_h-$7F_h$	**EPC_Private [47:32]**															
		60_h-$6F_h$	**EPC_Private [63:48]**															
		50_h-$5F_h$	**EPC_Private [79:64]**															
		40_h-$4F_h$	**EPC_Private [95:80]**															
		30_h-$3F_h$	**EPC_Private [111:96]**															
		20_h-$2F_h$	**EPC_Private [127:112]**															
		10_h-$1F_h$	**Protocol-Control Bits (PC)**															
		00_h-$0F_h$	**CRC-16**															
00_2	RESERVED (NVM)	30_h-$3F_h$	**Access Password[15:0]**															
		20_h-$2F_h$	**Access Password[31:16]**															
		10_h-$1F_h$	**Kill Password[15:0]**															
		00_h-$0F_h$	**Kill Password[31:16]**															

Table 4-2 Physical/Logical Memory Map–Monza 4QT (Public Mode)

Memory Bank Number	Memory Bank Name	Memory Bank Bit Address	Bit Number															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		10_h-$1F_h$	Manufacturer ID				Model Number											
		00_h-$0F_h$	1	1	1	0	0	0	1	0	Manufacturer ID							
01_2	EPC_Public (NVM / Write Locked)	70_h-$7F_h$	EPC_Public[15:0]															
		60_h-$6F_h$	EPC_Public [31:16]															
		50_h-$5F_h$	EPC_Public [47:32]															
		40_h-$4F_h$	EPC_Public [63:48]															
		30_h-$3F_h$	EPC_Public [79:64]															
		20_h-$2F_h$	EPC_Public [95:80]															
		10_h-$1F_h$	Protocol-Control Bits (PC)															
		00_h-$0F_h$	CRC-16															
00_2	RESERVED (NVM / R/W Locked)	30_h-$3F_h$	Access Password[15:0]															
		20_h-$2F_h$	Access Password[31:16]															
		10_h-$1F_h$	Kill Password[15:0]															
		00_h-$0F_h$	Kill Password[31:16]															

Table 4-3 Physical/Logical Memory Map–Monza 4E

Memory Bank Number	Memory Bank Name	Memory Bank Bit Address	Bit Number															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
11_2	User (NVM)	70_h-$7F_h$	User[15:0]															
		60_h-$6F_h$	User[31:16]															
		…	…															
		10_h-$1F_h$	User[111:96]															
		00_h-$0F_h$	User[127:112]															
10_2	TID (ROM)	50_h-$5F_h$	TID_Serial[15:0]															
		40_h-$4F_h$	TID_Serial[31:16]															
		30_h-$3F_h$	TID_Serial[47:32]															
		20_h-$2F_h$	Extended TID Header															
		10_h-$1F_h$	Manufacturer ID				Model Number											
		00_h-$0F_h$	1	1	1	0	0	0	1	0	Manufacturer ID							
01_2	EPC (NVM)	200_h-$20F_h$	EPC[15:0]															
		$1F0_h$-$1FF_h$	EPC[31:16]															
		$1E0_h$-$1EF_h$	EPC[47:32]															
		$1D0_h$-$1DF_h$	EPC[63:48]															
		…	…															
		40_h-$4F_h$	EPC[463:448]															
		30_h-$3F_h$	EPC[479:464]															
		20_h-$2F_h$	EPC[495:480]															
		10_h-$1F_h$	Protocol-Control Bits (PC)															
		00_h-$0F_h$	CRC-16															
00_2	RESERVED (NVM)	30_h-$3F_h$	Access Password[15:0]															
		20_h-$2F_h$	Access Password[31:16]															
		10_h-$1F_h$	Kill Password[15:0]															
		00_h-$0F_h$	Kill Password[31:16]															

Table 4-4 Physical/Logical Memory Map–Monza 4D

Memory Bank Number	Memory Bank Name	Memory Bank Bit Address	Bit Number															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
11_2	User (NVM)	10_h-$1F_h$	User[15:0]															
		00_h-$0F_h$	User[31:16]															
10_2	TID (ROM)	50_h-$5F_h$	TID_Serial[15:0]															
		40_h-$4F_h$	TID_Serial[31:16]															
		30_h-$3F_h$	TID_Serial[47:32]															
		20_h-$2F_h$	Extended TID Header															
		10_h-$1F_h$	Manufacturer ID				Model Number											
		00_h-$0F_h$	1	1	1	0	0	0	1	0	Manufacturer ID							
01_2	EPC (NVM)	90_h-$9F_h$	EPC[15:0]															
		80_h-$8F_h$	EPC[31:16]															
		70_h-$7F_h$	EPC[47:32]															
		60_h-$6F_h$	EPC[63:48]															
		50_h-$5F_h$	EPC[79:64]															
		40_h-$4F_h$	EPC[95:80]															
		30_h-$3F_h$	EPC[111:96]															
		20_h-$2F_h$	EPC[127:112]															
		10_h-$1F_h$	Protocol-Control Bits (PC)															
		00_h-$0F_h$	CRC-16															
00_2	RESERVED (NVM)	30_h-$3F_h$	Access Password[15:0]															
		20_h-$2F_h$	Access Password[31:16]															
		10_h-$1F_h$	Kill Password[15:0]															
		00_h-$0F_h$	Kill Password[31:16]															

4.2 Logical vs. Physical Bit Identification

For the purposes of distinguishing most significant from least significant bits, a logical representation is used in this datasheet where MSBs correspond to large bit numbers and LSBs to small bit numbers. For example, Bit 15 is the logical MSB of a memory row in the memory map. Bit 0 is the LSB. A multi-bit word represented by WORD[N:0] is interpreted as MSB first when read from left to right. This convention should not be confused with the physical bit address indicated by the rows and column addresses in the memory map; the physical bit address describes the addressing used to access the memory.

4.3 Memory Banks

Described in the following sections are the contents of the NVM and ROM memory, and the parameters for their associated bit settings.

4.3.1 Reserved Memory

Reserved Memory contains the *Access* and *Kill* passwords.

4.3.2 Passwords

Monza 4 tag chips have a 32-bit Access Password and 32-bit Kill Password. The default password for both Kill and Access is $00000000_{h.}$

4.3.2.1 Access Password

The Access Password is a 32-bit value stored in Reserved Memory 20_h to $3F_h$ MSB first. The default value is all zeroes. Tags with a non-zero Access Password will require a reader to issue this password before transitioning to the secured state. A tag that does not implement an Access Password acts as though it had a zero-valued Access Password that is permanently read/write locked.

4.3.2.2 Kill Password

The Kill Password is a 32-bit value stored in Reserve Memory 00_h to $1F_{h,}$ MSB first. The default value is all zeroes. A reader shall use a tag's kill password once to kill the tag and render it silent thereafter. A tag will not execute a kill operation if its Kill Password is all zeroes. A tag that does not implement a Kill Password acts as though it had a zero-valued Kill Password that is permanently read/write locked.

4.3.3 EPC Memory (EPC data, Protocol Control Bits, and CRC16)

As per the Gen 2 specification, EPC memory contains a 16 bit cyclic-redundancy check word (CRC16) at memory addresses 00_h to $0F_h$, the 16 protocol-control bits (PC) at memory addresses 10_h to $1F_h$, and an EPC value beginning at address 20_h.

The protocol control fields include a five-bit EPC length, a one-bit user-memory indicator (UMI), a one-bit extended protocol control indicator, and a nine-bit numbering system identifier (NSI). The default (unprogrammed) value is 0000_h.

The tag calculates the CRC16 upon power-up over the stored PC bits and the EPC specified by the EPC length field in the stored PC. For more details about the PC field or the CRC16, see the Gen 2 specification.

A reader accesses EPC memory by setting MemBank = 01_2 in the appropriate command, and providing a memory address using the extensible-bit-vector (EBV) format. The CRC-16, PC, and EPC are stored MSB first (i.e., the EPC's MSB is stored in location 20_h).

For Monza 4QT tag chip models, the EPC memory contains a 96-bit, write-locked EPC in the Public mode, and a 128-bit EPC in the Private mode. For Monza 4QT chips (IPJ-W1502), the EPC value listed below is for the Private profile only.

The EPC written at time of manufacture is as shown in Table 4-5.

Table 4-5 EPC at Manufacture

Impinj Part Number	Protocol-Control Bits at Memory Addresses 10_h to $1F_h$	EPC Value Pre-programmed at Manufacture (hex)[1]
IPJ-W1510 IPJ-W1512 IPJ-W1513	0011 0000 0000 0000	3008 33B2 DDD9 0140 0000 0000

Note 1: The EPC is factory encoded with 96 bits to ensure backward compatibility with older readers. Users must encode Monza 4 tag chips above 96 bits.

Tag Identification (TID) Memory

The ROM-based Tag Identification memory contains Impinj-specific data. The Impinj MDID (Manufacturer Identifier) for Monza 4 is 100000000001 (the location of the manufacturer ID is shown in the memory map tables above, and the bit details are given in Table 4-6). Note that a logic 1 in the most significant bit of the manufacturer ID (as in the example bordered in solid black in the table) indicates the presence of an extended TID consisting of a 16-bit header and a 48-bit serialization. The Monza 4 tag chip model number is located in the area bordered by the dashed line in TID memory row 10_h-$1F_h$ as shown in Table 4-1 through Table 4-4. See Table 4-7 for a list of the Monza 4 model numbers. The non-shaded bit locations in TID row 00_h-$0F_h$ store the EPCglobal™ Class ID (0xE2).

Table 4-6 TID Memory Details

Memory Bank Description	Memory Bank Bit Address	Bit Number															
10_2 TID (ROM)	50_h-$5F_h$	TID_SERIAL[15:0]															
	40_h-$4F_h$	TID_SERIAL[31:16]															
	30_h-$3F_h$	TID_SERIAL[47:32]															
	20_h-$2F_h$	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	10_h-$1F_h$	0	0	0	1	Model Number (See Table 4-7)											
	00_h-$0F_h$	1	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0

Table 4-7 Monza 4 Model Numbers

Model	Model Number
Monza 4QT	000100000101
Monza 4E	000100001100
Monza 4D	000100000000

5 Absolute Maximum Ratings

Stresses beyond those listed in this section may cause permanent damage to the tag. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this datasheet is not guaranteed or implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.1 Temperature

Several different temperature ranges will apply over unique operating and survival conditions. Table 5-1 lists the ranges that will be referred to in this specification. Tag functional and performance requirements are met over the operating range, unless otherwise specified.

Table 5-1 Temperature parameters

Parameter	Minimum	Typical	Maximum	Units	Comments
Extended Operating Temperature	–40		+85	°C	Default range for all functional and performance requirements
Storage Temperature	–40		+85	°C	
Assembly Survival Temperature			+150	°C	Applied for one minute
Temperature Rate of Change			4	°C / sec	During operation

5.2 Electrostatic Discharge (ESD) Tolerance

The tag is guaranteed to survive ESD as specified in Table 5-2.

Table 5-2 ESD Limits

Parameter	Minimum	Typical	Maximum	Units	Comments
ESD			2,000	V	HBM (Human Body Model)

5.3 NVM Use Model

Tag memory is designed to endure 100,000 write cycles or retain data for 50 years.

6 Ordering Information

Contact RFID_sales@impinj.com for ordering support.

Part Number	Form	Product	Processing Flow[1]
IPJ-W1510-A00 IPJ-W1512-A00 IPJ-W1513-A00	Wafer	Monza 4E tag chip Monza 4QT tag chip Monza 4D tag chip	Tested only: non-bumped, non-thinned (~700 µm wafer thickness)
IPJ-W1510-C00, IPJ-W1512-C00, IPJ-W1513-C00	Wafer	Monza 4E tag chip Monza 4QT tag chip Monza 4D tag chip	Bumped, thinned (to 3 mils, or ~75 µm wafer thickness), and diced

Note 1: See Monza 4 Wafer Specification for further details.

Notices:

This product is covered by one or more of the following U.S. patents. Other patents pending. 7283037, 7026935, 7049964, 7501953, 7030786, 7246751, 7245213, 7408466, 7187290, 7215251, 7116240, 7183926, 7312622, 7307528, 7388468, 7394324, 7120550, 7253719, 7380190, 7403122, 7307529, 7472835, 7561866, 7405659, 7307534, 7528728, 7423539, 7123171, 7420469, 7541843, 7448547, 7525438, 7482251

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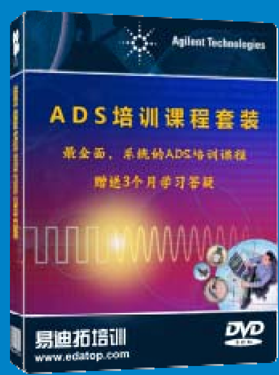
该套装是迄今国内最全面、最权威的 ADS 培训教程，共包含 10 门 ADS 学习培训课程。课程是由具有多年 ADS 使用经验的微波射频与通信系统设计领域资深专家讲解，并多结合设计实例，由浅入深、详细而又全面地讲解了 ADS 在微波射频电路设计、通信系统设计和电磁仿真设计方面的内容。能让您在最短的时间内学会使用 ADS，迅速提升个人技术能力，把 ADS 真正应用到实际研发工作中去，成为 ADS 设计专家...

课程网址： http://www.edatop.com/peixun/ads/13.html



HFSS 学习培训课程套装

该套课程套装包含了本站全部 HFSS 培训课程，是迄今国内最全面、最专业的 HFSS 培训教程套装，可以帮助您从零开始，全面深入学习 HFSS 的各项功能和在多个方面的工程应用。购买套装，更可超值赠送 3 个月免费学习答疑，随时解答您学习过程中遇到的棘手问题，让您的 HFSS 学习更加轻松顺畅…

课程网址：http://www.edatop.com/peixun/hfss/11.html

CST 学习培训课程套装

该培训套装由易迪拓培训联合微波 EDA 网共同推出，是最全面、系统、专业的 CST 微波工作室培训课程套装，所有课程都由经验丰富的专家授课，视频教学，可以帮助您从零开始，全面系统地学习 CST 微波工作的各项功能及其在微波射频、天线设计等领域的设计应用。且购买该套装，还可超值赠送 3 个月免费学习答疑…

课程网址：http://www.edatop.com/peixun/cst/24.html

HFSS 天线设计培训课程套装

套装包含 6 门视频课程和 1 本图书，课程从基础讲起，内容由浅入深，理论介绍和实际操作讲解相结合，全面系统的讲解了 HFSS 天线设计的全过程。是国内最全面、最专业的 HFSS 天线设计课程，可以帮助您快速学习掌握如何使用 HFSS 设计天线，让天线设计不再难…

课程网址：http://www.edatop.com/peixun/hfss/122.html

13.56MHz NFC/RFID 线圈天线设计培训课程套装

套装包含 4 门视频培训课程，培训将 13.56MHz 线圈天线设计原理和仿真设计实践相结合，全面系统地讲解了 13.56MHz 线圈天线的工作原理、设计方法、设计考量以及使用 HFSS 和 CST 仿真分析线圈天线的具体操作，同时还介绍了 13.56MHz 线圈天线匹配电路的设计和调试。通过该套课程的学习，可以帮助您快速学习掌握 13.56MHz 线圈天线及其匹配电路的原理、设计和调试…

详情浏览：http://www.edatop.com/peixun/antenna/116.html

我们的课程优势：

※ 成立于 2004 年，10 多年丰富的行业经验，

※ 一直致力并专注于微波射频和天线设计工程师的培养，更了解该行业对人才的要求

※ 经验丰富的一线资深工程师讲授，结合实际工程案例，直观、实用、易学

联系我们：

※ 易迪拓培训官网：http://www.edatop.com

※ 微波 EDA 网：http://www.mweda.com

※ 官方淘宝店：http://shop36920890.taobao.com